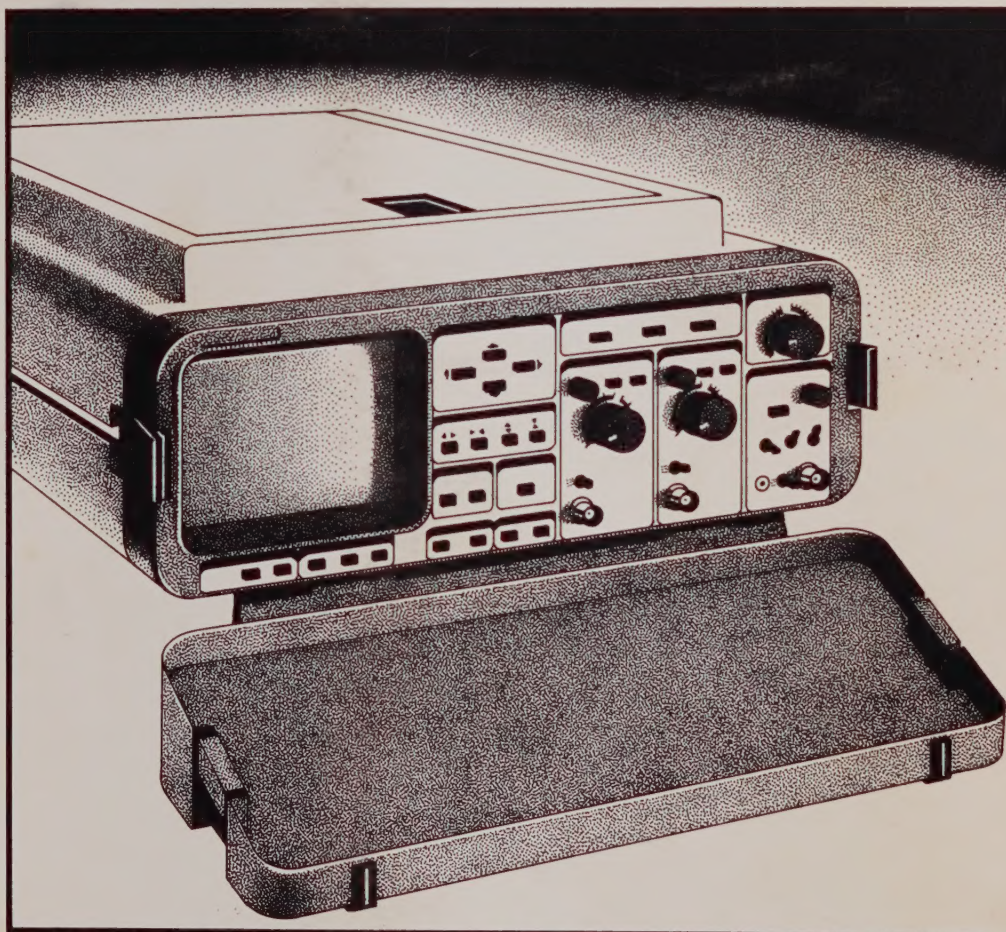


Electronic Services - Hayward, Ca
M19578X



 Nicolet

PART # 269-900900



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INTRODUCTION

WARNING: The service instructions in this manual are for qualified personnel only. High voltages exist within this instrument.

Before servicing the instrument, read the Caution Notes on page 4-1, then the procedure to be performed. If any questions arise, contact -

Nicolet Instrument Corporation
Oscilloscope Division, Service Dept.
Madison, Wisconsin 53711
Telephone (608) 273-5010

CAUTION: Read the Power Requirements, page 5-1 before applying power to the instrument.

► **IMPORTANT:** Data stored in the display memory will be lost if any of the following occurs-

- #1. New data is captured by the instrument.
- #2. Data is read from a Bubble Memory block into an activate channel.
- #3. A "saved" memory section copies data from its respective channel.
- #4. A function is executed that replaces data in display memory with its result. (See the Operation manual, Section 13).
- #5. Power is removed from the instrument.

RECEIVING

Unpack the instrument and save the carton and packing material in case the instrument must be shipped to another site or returned to the factory for service.

INSPECTION

Inspect the exterior of the instrument for any visible signs of damage that may have occurred during transit.

If damaged, call Nicolet Oscilloscope Division, Shipping Department at (608) 271-3333 for instructions.

Outside the U.S., call your local Nicolet office or distributor.

CAUTIONS

The following information is required by the FCC and relates only to the interference potential of this equipment. This message is a direct quotation. Although stated as a "Warning," there is essentially no risk of injury, loss of life, or equipment damage.

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J or Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

CAUTION: This instrument and related accessories are not designed for biomedical experiments on humans and should not be directly connected to human subjects.

CAUTION: This instrument must not be operated in explosive atmospheres.

WARNING: High voltages exist in this instrument. Use a non-conductive, nonmetallic alignment tool when aligning the instrument.

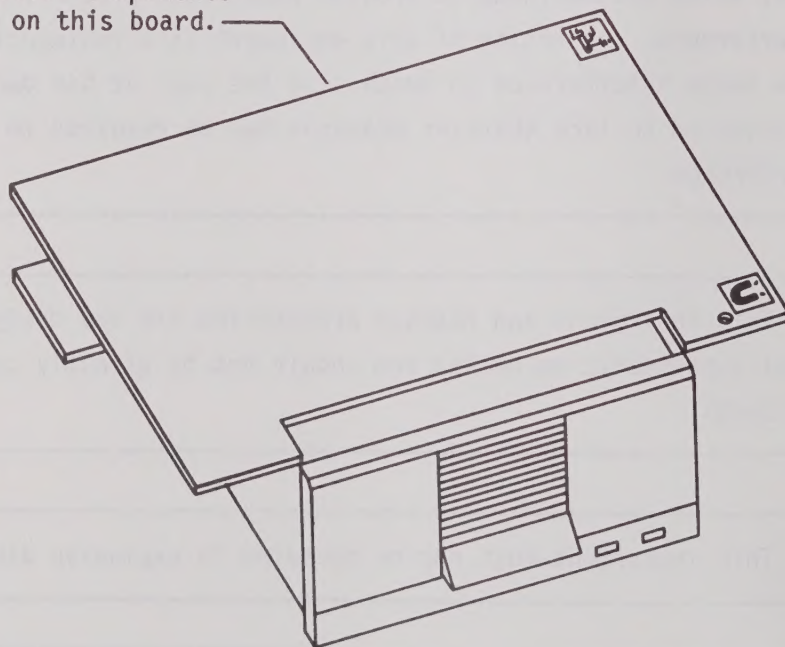
WARNING: Refer to Section 5, page 5-1 (Power Requirements) before applying power to the instrument.

CAUTION: Ensure that the input signal does not exceed the maximum allowable input voltage, with respect to ground, listed in Section #6 (Specifications).

CAUTION: Remove all power from the instrument before removing its covers.

CAUTION: The bubble memory is equipped with static sensitive components (Figure 4-1). Ensure that you are properly grounded before servicing the instrument to guard against component damage.

Static sensitive components are mounted on this board.



CAUTION: The bubble memory assembly contains static sensitive components. Ensure that you are properly grounded before servicing the instrument to avoid component damage.

Figure 4-1

POWER REQUIREMENTS

The power requirement of this instrument is nominally 90 watts. It is designed to operate from either of these single phase, ac voltage power ranges only: 90 to 132 vac, or 180 to 264 vac (47 to 440 Hz).

WARNING: Inspect the voltage selector (Figure 5-1) at the rear of the instrument for the correct setting before applying power.

EXAMPLE 5-1

The power selector is set for 120 vac in Figure 5-1.

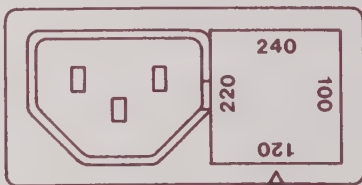


Figure 5-1

INPUT VOLTAGE SELECTIONS (120V/240V)

CAUTION: Remove all power from the instrument before continuing.

- #1. Remove the power cord from the instrument's rear panel receptacle.
- #2. Use a small screwdriver and carefully pry the voltage selector from the power receptacle module, (Figure 5-2).
- #3. Install the voltage selector with the correct voltage range (**120V or 240V**) marked on the power selector pointed towards the bottom of the scope.

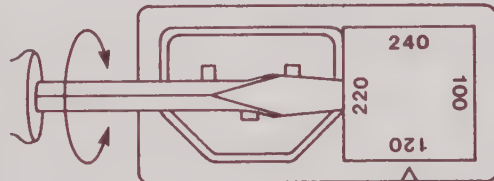


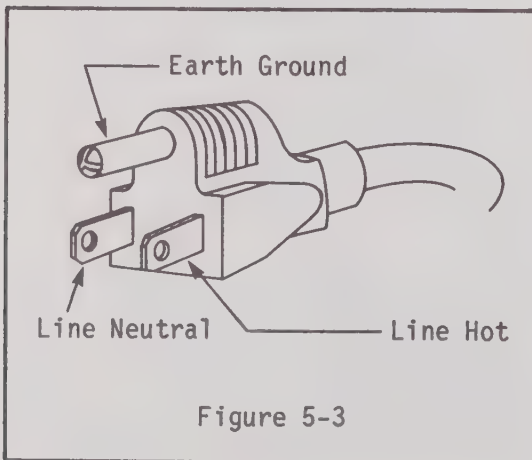
Figure 5-2

POWER SOURCE REQUIREMENTS

The power source must include:

- #1. A neutral wire at or near ground potential.
- #2. A separate safety ground at ground potential.
- #3. A line (hot) wire.

Figure 5-3 illustrates the locations of the neutral, line, and earth ground terminals located on the male connector of a U.S. power cord. In other countries, refer to local codes.



REPLACING THE LINE FUSE

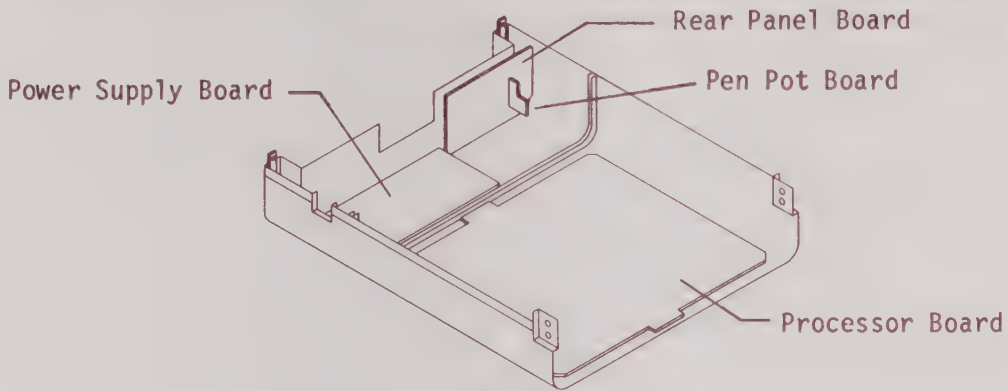
CAUTION: Remove all power from the instrument before continuing.

- #1. Remove the power cord from the instrument's rear panel receptacle.
- #2. Use a small screwdriver and carefully pry the voltage selector from the power receptacle module, (Figure 5-2, page 5-1).
- #3. Replace the fuse with a 3 amp, 250 volt slow blow fuse and install the power selector with the correct power range (**120V or 240V**) pointed towards the bottom of the instrument.

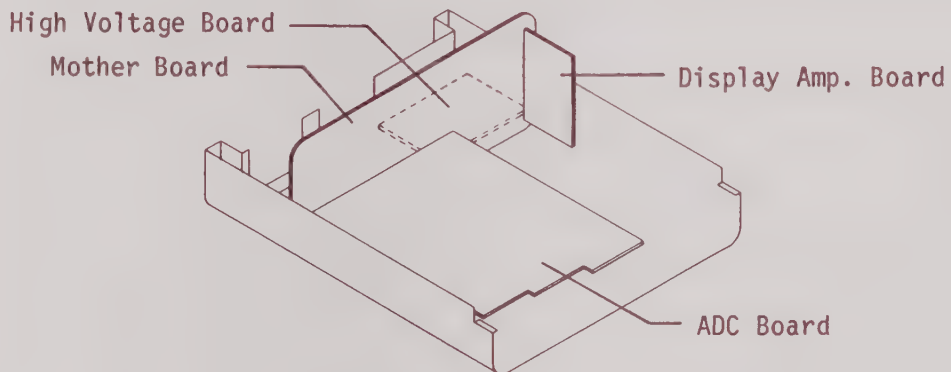
SPECIFICATIONS

The NIC-320 specifications are located in the rear cover pocket of this manual.

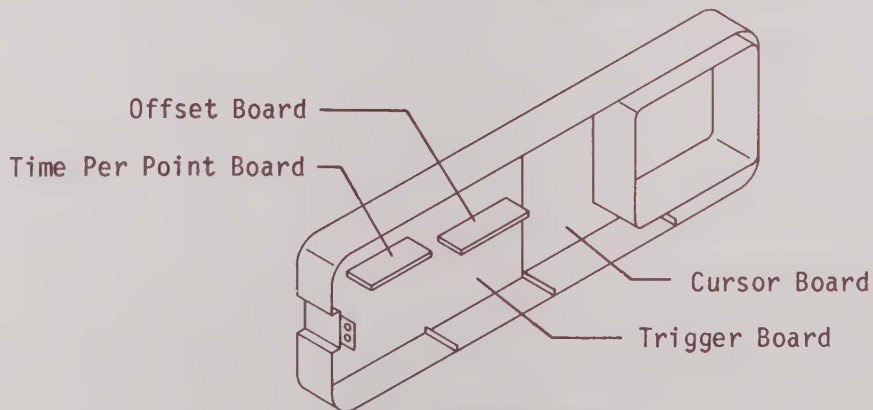
320 ASSEMBLY IDENTIFICATION



BOTTOM COVER

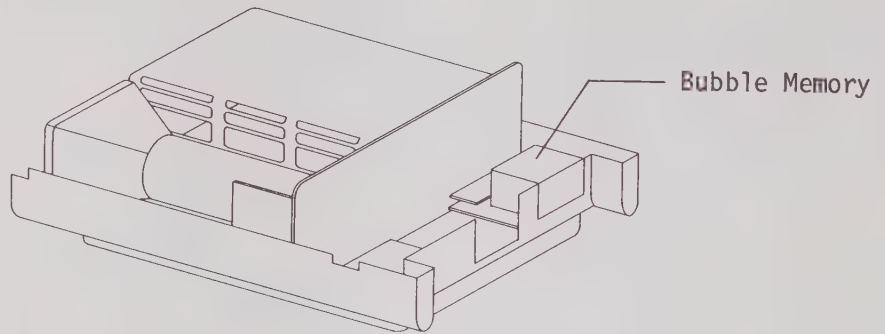


TOP COVER



FRONT PANEL

ACCESSORIES



TOP COVER

DISASSEMBLY PROCEDURES

This section describes the disassembly procedures listed in Index 8-1.

► **IMPORTANT:** Review the Caution Notes (Section #4) before servicing the instrument. If any questions arise while servicing the instrument, contact -

Nicolet Instruments Corporation
Oscilloscope Division, Service Dept.
Madison, Wisconsin 53711
Telephone (608) 273-5010

TOOLS REQUIRED

- #1. Phillips screwdriver.
- #2. Soldering iron (when required).

DISASSEMBLY PROCEDURE	PAGE
Separating the Covers	8-3
Trigger Board	8-5
Offset Board	8-5
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Power Supply Board	8-13
CRT Display	8-14

Table 8-1

SEPARATING THE COVERS

This procedure removes the front panel assembly and separates the covers. Do not perform this procedure unless directed to do so.

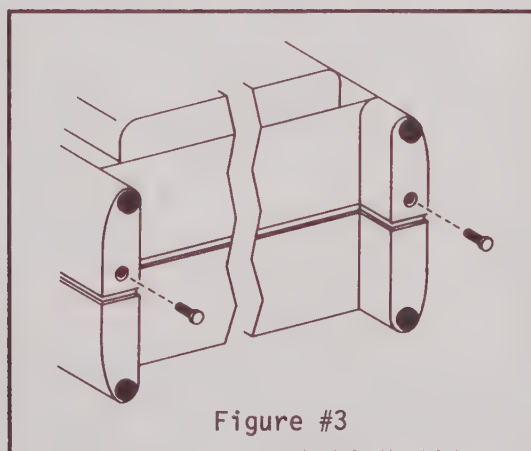
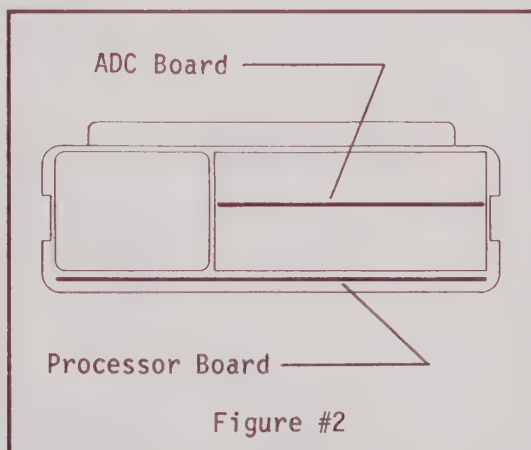
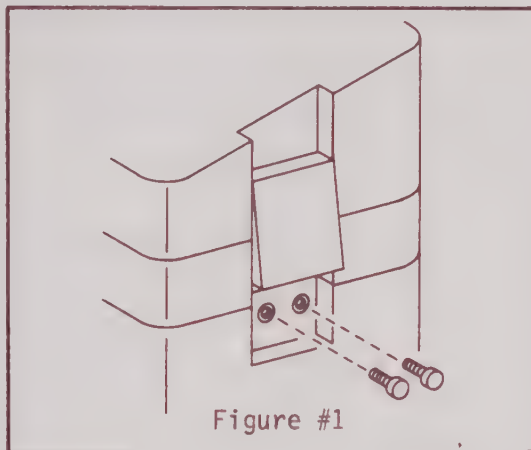
CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Latch the front cover to the panel assembly and stand the instrument on its rear panel.
- #2. Remove the front cover securing screws (Figure #1).
- #3. Carefully pull the front panel and cover assembly from the instrument and set it aside.
- #4. Pull the ADC and Processor boards out of the instrument (Figure #2).
- #5. Turn the instrument over to rest on its top cover.
- #6. Remove the two securing screws from the rear of the instrument, (Figure #3).

CAUTION: Perform steps 7, 8, and 9 with care, wires are connected inside the instrument.

- #7. Carefully separate the covers by loosening the front ends and then the back ends alternately.



#8. Raise the rear of the upper cover and disconnect the ribbon cable from the Rear Panel board at point (A), Figure #4.

#9. Raise the rear of the upper cover and disconnect the power cable from the Mother board at point (B), Figure #4. Set the upper cover aside.

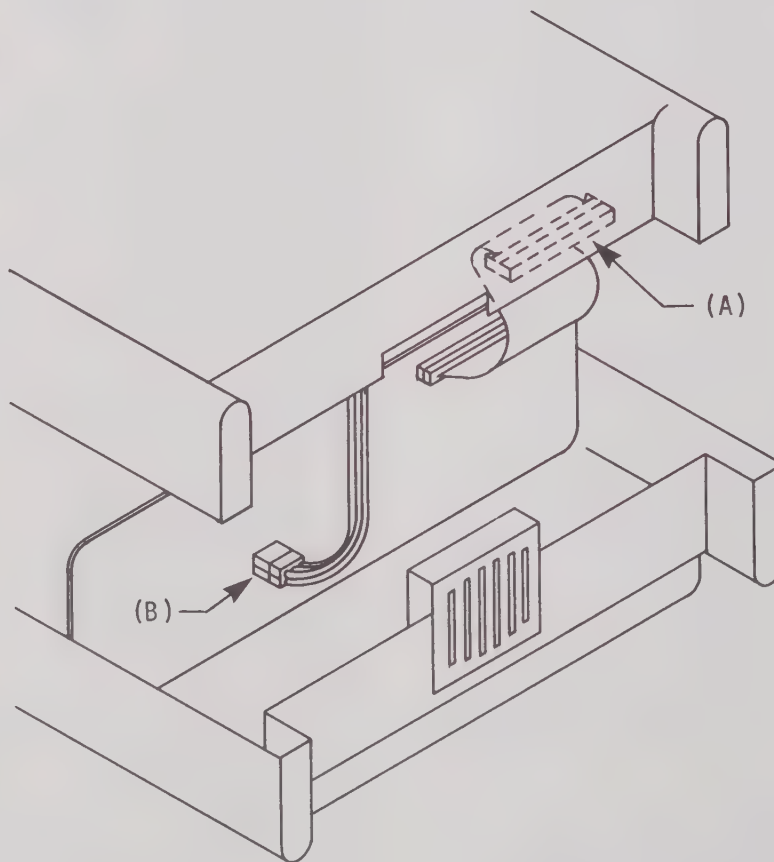


Figure #4

TRIGGER, TPP, OFFSET, CURSOR BOARDS

This procedure accesses the Trigger, Time Per Point, Offset, and Cursor boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Unsnap the front cover latches and pull off the front panel, rotary control knobs.
- #2. Latch the front cover to the front panel assembly and stand the instrument on its rear panel.
- #3. Remove the front panel securing screws (Figure #1).
- #4. Carefully pull the front panel assembly from the instrument.
- #5. Refer to Figure #2 and remove the mounting screws as required to remove the desired board(s).

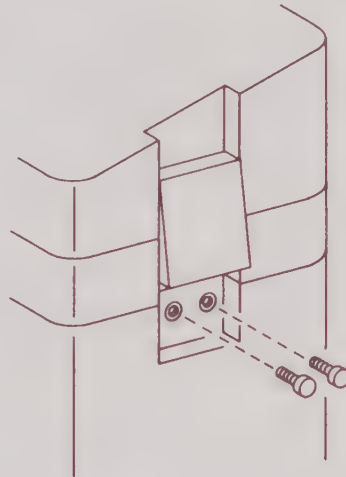


Figure #1

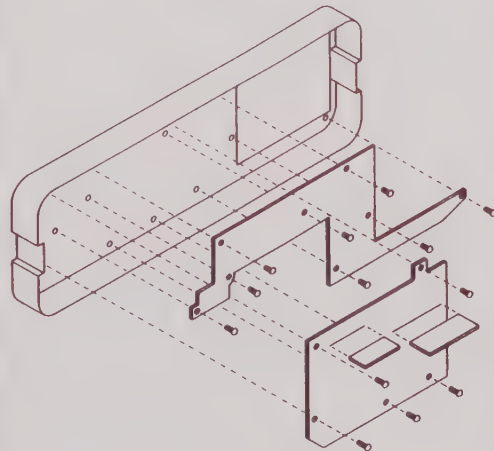


Figure #2

REMOVING THE ADC/PROCESSOR BOARDS

This procedure removes the ADC and/or Processor boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

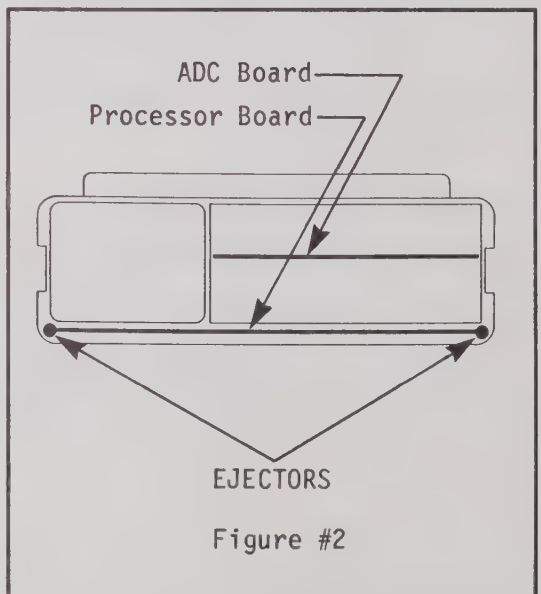
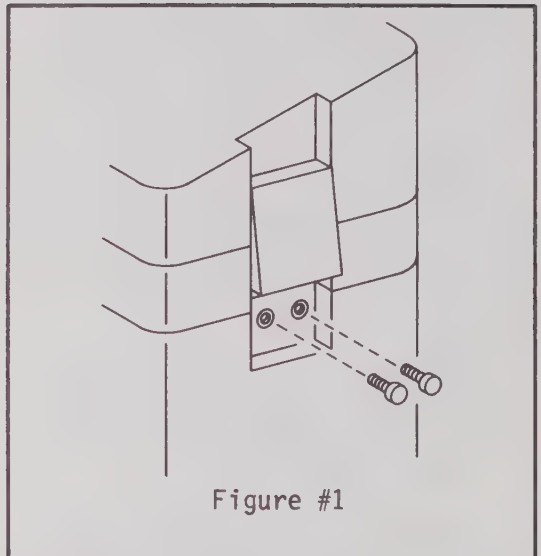
- #1. Latch the front cover to the front panel assembly and stand the instrument on its rear panel.
- #2. Remove the front panel securing screws (Figure #1).
- #3. Carefully pull the front panel assembly from the instrument and set it aside.

To Remove the ADC Board

- #4a. Slide the ADC board out of the card cage (Figure #2) and set it aside.

To Remove the Processor Board

- #4b. Pull the Processor board (Figure #2) out of the instrument using the two board ejectors.



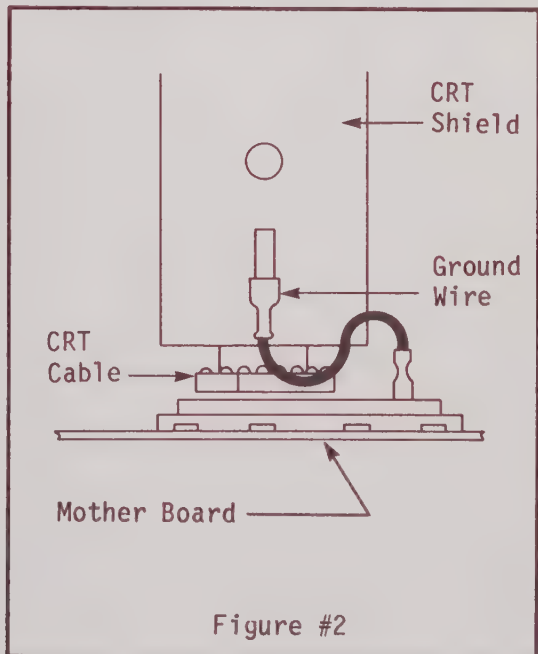
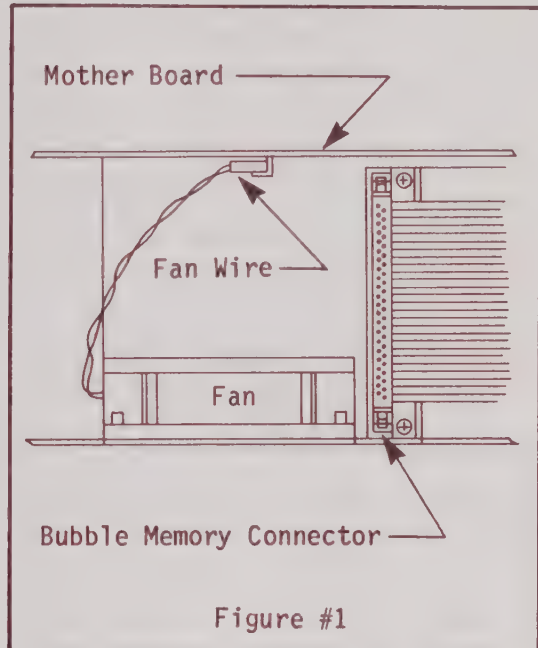
REMOVING THE MOTHER/DISPLAY AMP. BOARD

This procedure removes the Mother and Display Amplifier boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Separate the covers, (page 8-3).
- #2. If the Bubble Memory accessory is installed, unplug the ribbon cable from the Bubble Memory board (Figure #1).
- #3. Unplug the fan wire from the Mother board (Figure #1).
- #4. Unplug the ground wire from the CRT shield (Figure #2).
- #5. Unplug the CRT cable (Figure #2) from the rear of the CRT display.



- #6. Carefully slide the CRT forward until the high voltage anode plug (Figure #3) can be accessed and unplug the wire.

WARNING: Remove the CRT with care and set it aside.

- #7. Disconnect the six CRT connector wires from the High Voltage board (Figure #4).
- #8. Remove the Mother board (Figure #4) and set it aside.

NOTE: Free the high voltage anode wire from the wire holder on top of the crt shield.

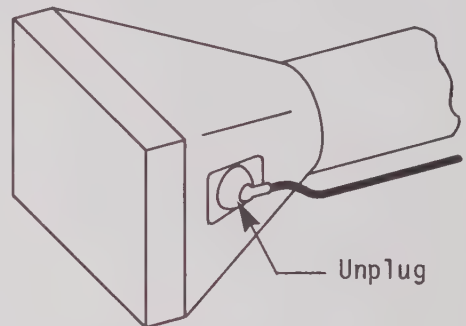


Figure #3

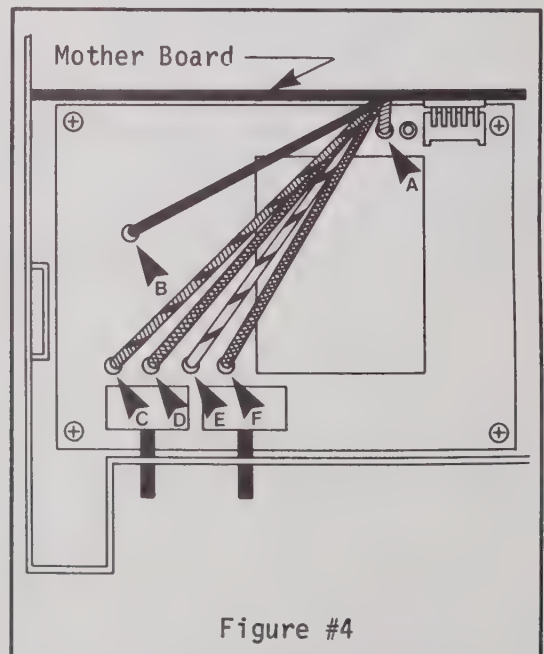


Figure #4

REMOVING THE HIGH VOLTAGE BOARD

This procedure removes the High Voltage board.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Remove the Mother & Display Amp boards (page 8-7).

CAUTION: Be sure to remove the crt during the above procedure to prevent accidental droppage.

- #2. Remove the High Voltage board securing screws from each of its corners, then remove the board.

REMOVING THE REAR PANEL/PEN POT BOARDS

This procedure removes the Rear Panel and Pen Pot boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Separate the covers, (page 8-3).
- #2. Remove the two RS-232 connector securing nuts (Figure #1).
- #3. Loosen the Pen Speed pot knob set screw and set the knob aside (Figure #1).
- #4. Remove the securing screws from the four corners of the Rear Panel board.

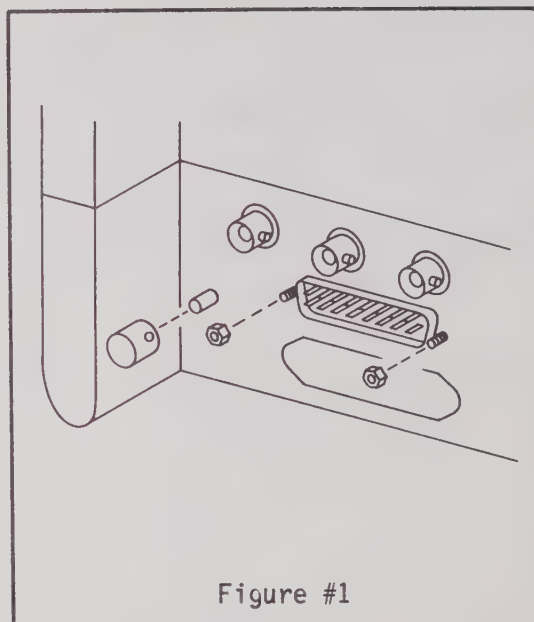


Figure #1

REMOVING THE EXTERNAL CONTROL BOARD

This procedure removes the External Control accessory board.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Separate the covers, (page 8-3).
- #2. Unplug the External Control board from the Mother board (Figure #1).

(Not Available At This Time)

Figure #1

REMOVING THE BUBBLE MEMORY HOLDER

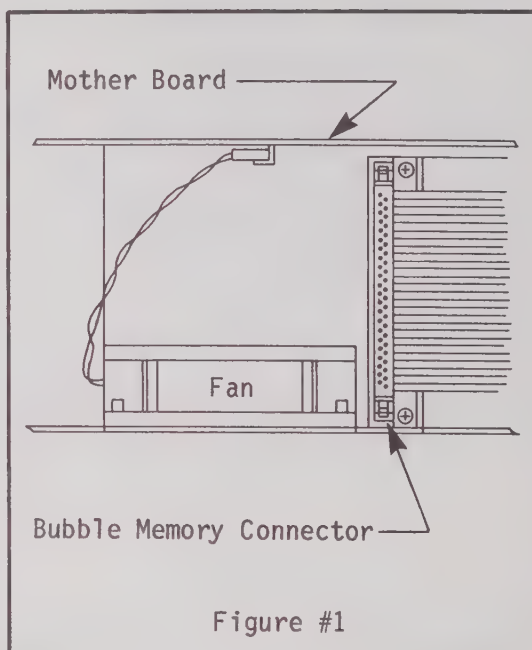
This procedure removes the Bubble Memory.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

CAUTION: The bubble memory is equipped with static sensitive components. You must be properly grounded before servicing the instrument to guard against component damage.

- #1. Separate the covers, (page 8-3).
- #2. Unplug the Bubble Memory ribbon cable from the Bubble Memory, (Figure #1).
- #3. Remove the Bubble Memory holder securing screws. Remove the Bubble Memory holder and set it aside on a static-free surface.



REMOVING THE POWER SUPPLY

This procedure removes the Power Supply.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Separate the covers, (page 8-3).
- #2. Free the Power ON/OFF switch from the cover (Figure #1).

- #3. Unplug all six wires from the fuse holder (Figure #1).
- #4. Remove the Grounding Lug (Figure #1).
- #5. Remove the five Power Supply securing screws and lift out the power supply shield and board.

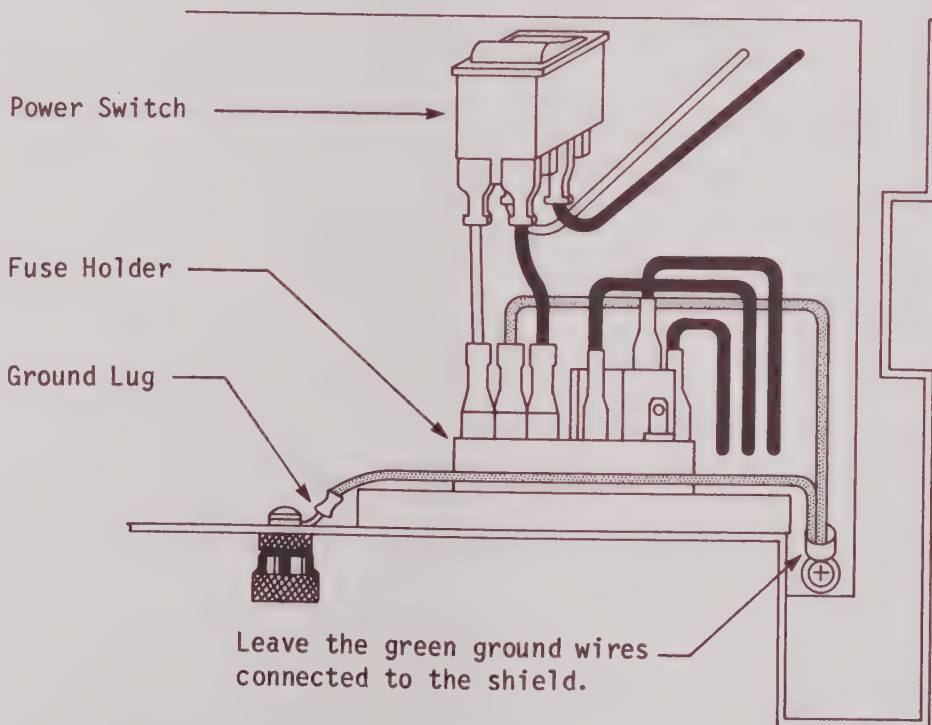


Figure #1

REMOVING THE CRT DISPLAY

This procedure removes the CRT display.

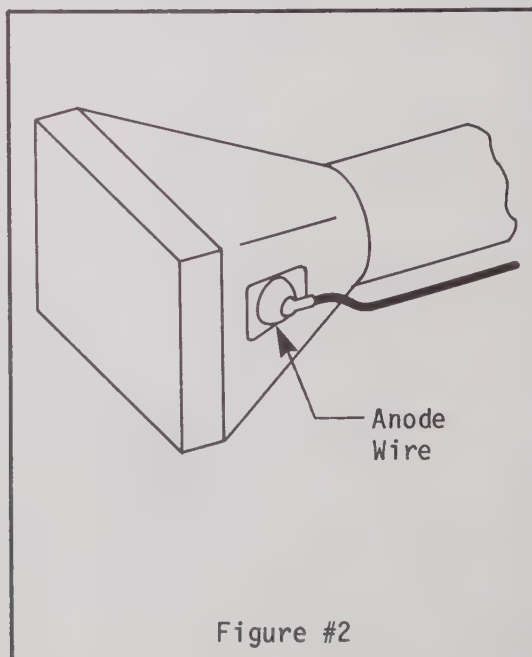
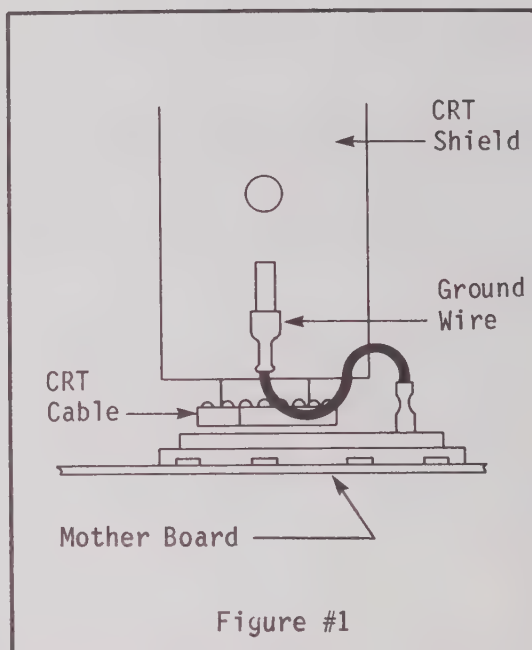
CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Separate the covers, (page 8-3).
- #2. Unplug the CRT shield ground wire (Figure #1).
- #3. Unplug the CRT connector from the rear of the CRT (Figure #1).

WARNING: Perform the next two steps with care.

- #4. Pull the CRT out from the front until the CRT High Voltage Anode wire can be accessed and unplug the anode wire from the CRT (Figure #2).
- #5. Carefully pull the CRT from its shield and set it aside.



REASSEMBLY PROCEDURES

This section describes the reassembly procedures listed in Index 9-1.

► **IMPORTANT:** Review the Caution Notes (Section #4) before servicing the instrument. If any questions arise while servicing the instrument, contact -

Nicolet Instruments Corporation
Oscilloscope Division, Service Dept.
Madison, Wisconsin 53711
Telephone (608) 273-5010

TOOLS REQUIRED

- #1. Phillips screwdriver.
- #2. Soldering iron (when required).

REASSEMBLY PROCEDURE	PAGE
Top & Bottom Covers	9-3
Front Panel	9-5
Trigger Board	9-5
Offset Board	9-6
Time Per Point Board	9-6
Cursor Board	9-6
ADC Board	9-6
Processor Board	9-6
Mother Board	9-7
Display Amp. Board	9-7
High Voltage Board	9-8
Rear Panel Board	9-10
Pen Pot Board	9-10
External Control Board	9-11
Bubble Memory	9-12
Power Supply Board	9-13
CRT Display	9-15

Index 9-1

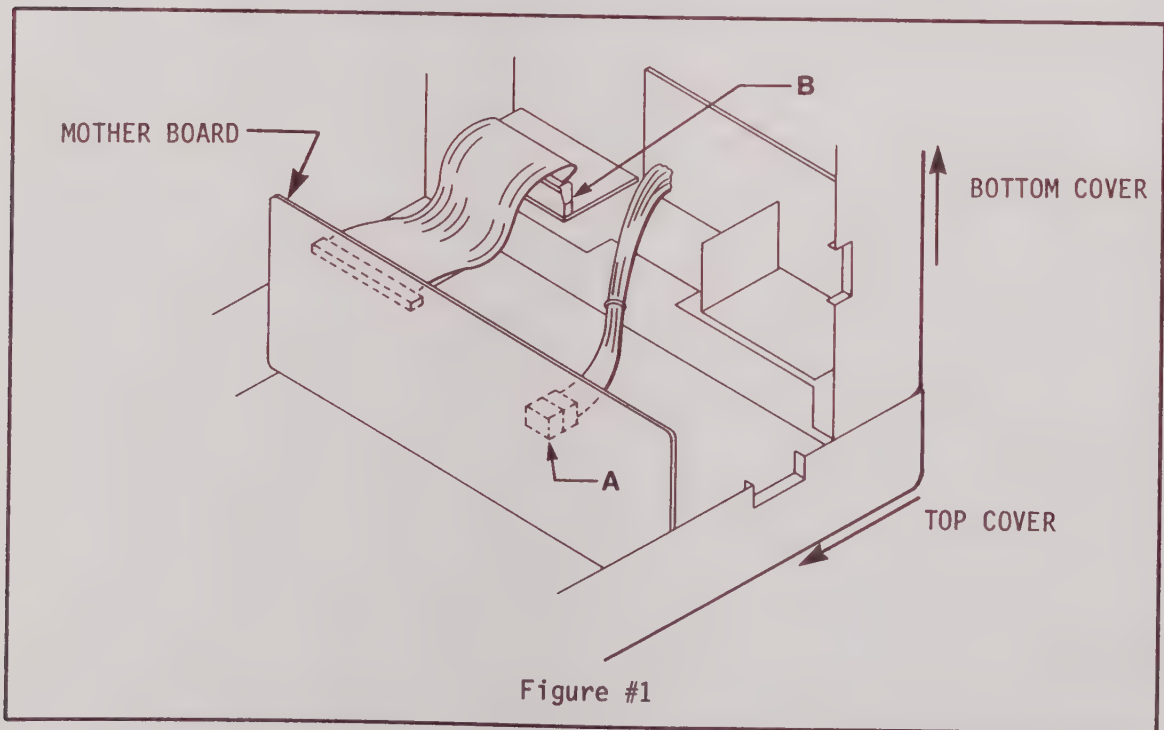
INSTALLING THE COVERS

This procedure reassembles the top and bottom covers.

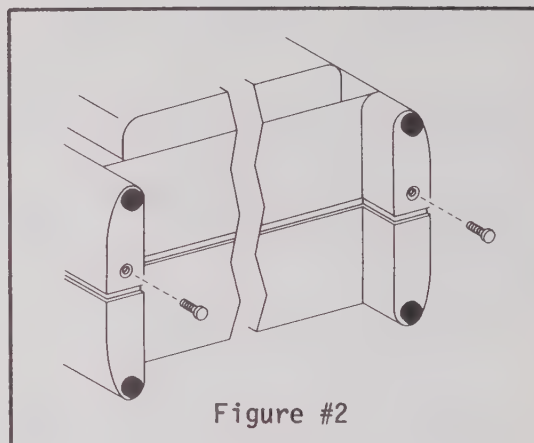
CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Turn the top cover over to rest on its top.
- #2. Inspect the top and bottom covers and insure that the CRT and all of the boards (**except the ADC and Processor boards**) are installed and secured.
- #3. Inspect all of the wires/cables for proper connections.
- #4. Set the bottom panel towards the rear of the top panel and connect the power cable to point (A) and (if applicable) the bubble memory connector to point (B), (Figure #1).



- #5. Mount the bottom panel to the top panel and secure with two securing screws (Figure #2).
- #6. Install the ADC and Processor boards (page 9-6)
- #7. Install the front panel assembly (page 9-5).



INSTALLING THE FRONT PANEL ASSEMBLY

This procedure installs the front panel assembly including the Trigger, TPP, Offset, and Cursor boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. If the top and bottom covers were separated, perform the procedure on page 9-3 before continuing.
- #2. Assemble and secure the front panel board(s) to the front panel assembly (Figure #1).
- #3. Clean the display screen with a mild detergent and a soft, damp cloth.
- #4. Mount the front panel assembly to the instrument.
- #5. Secure the front panel with four securing screws, two per side (Figure #2).
- #6. Replace the front panel rotary control knobs.

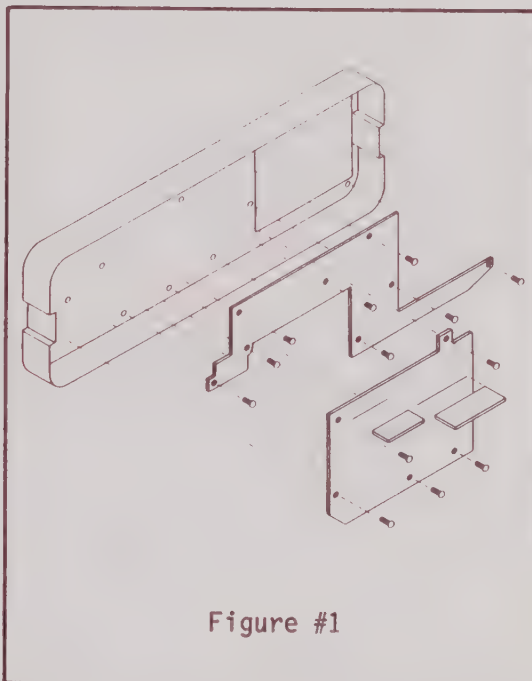


Figure #1

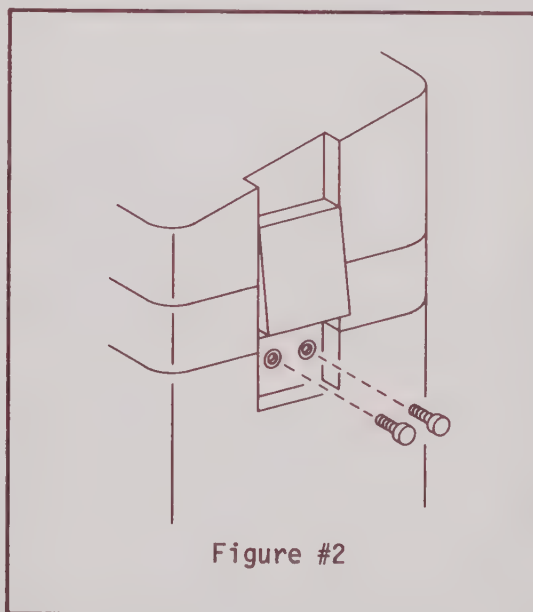


Figure #2

INSTALLING THE ADC/PROCESSOR BOARDS

This procedure installs the ADC and Processor boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

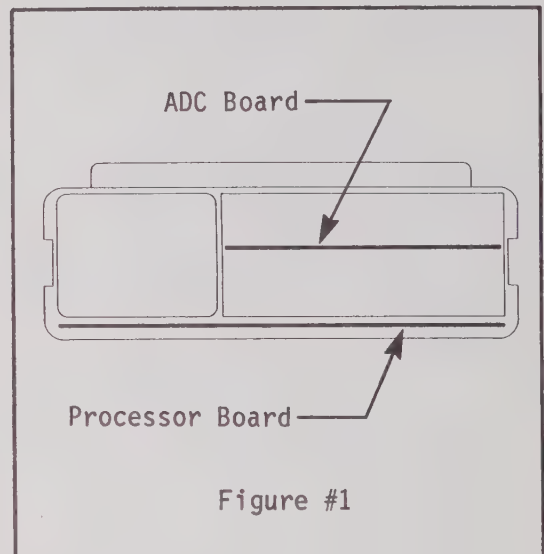
- #1. If the top and bottom covers are separated, perform the procedure on page 9-3 before continuing.

To Install the ADC Board

- #2a. Slide the ADC board with its component side towards the top cover into the printed circuit board cage until it mates with the Mother board connector (Figure #1).

To Install the Processor Board

- #2b. Slide the Processor board with its component side towards the top cover into the instrument until it mates with the Mother board connector (Figure #1).



INSTALLING THE MOTHER/DISPLAY AMP. BOARD

This procedure installs the Mother and Display Amplifier boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

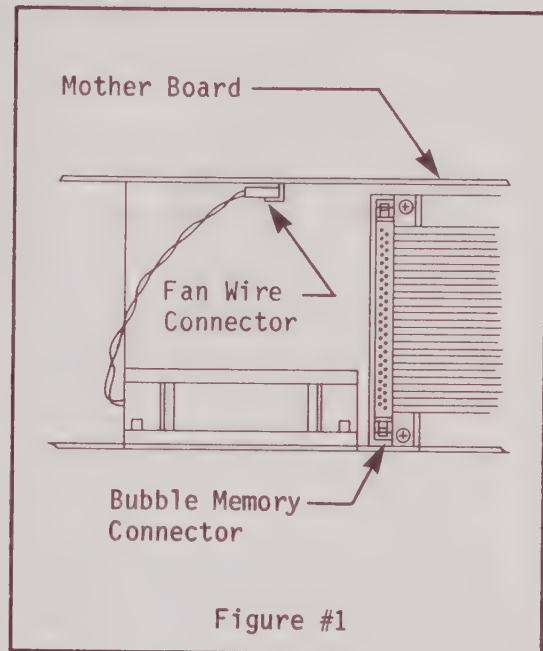
CAUTION: The bubble memory board contains static sensitive components, ground yourself before proceeding.

PROCEDURE

- #1. If applicable, install and secure the Bubble Memory holder (page 9-12).
- #2. Plug in the fan wire to the Mother board (Figure #1).

NOTE: Install the Rear Panel board if it was removed before continuing (page 9-10).

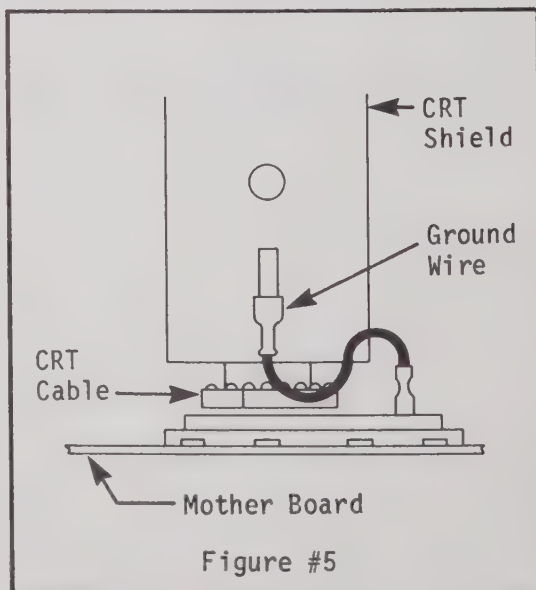
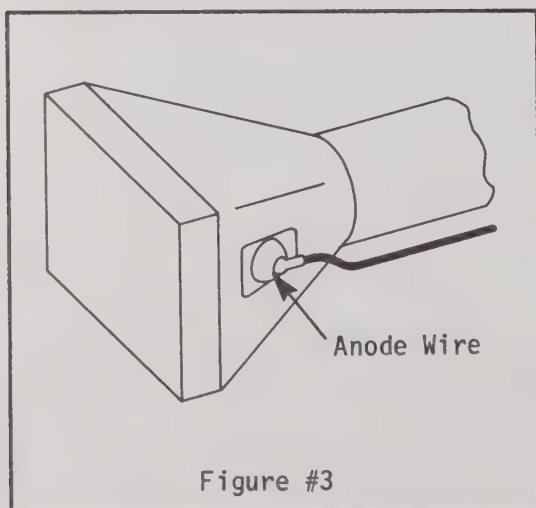
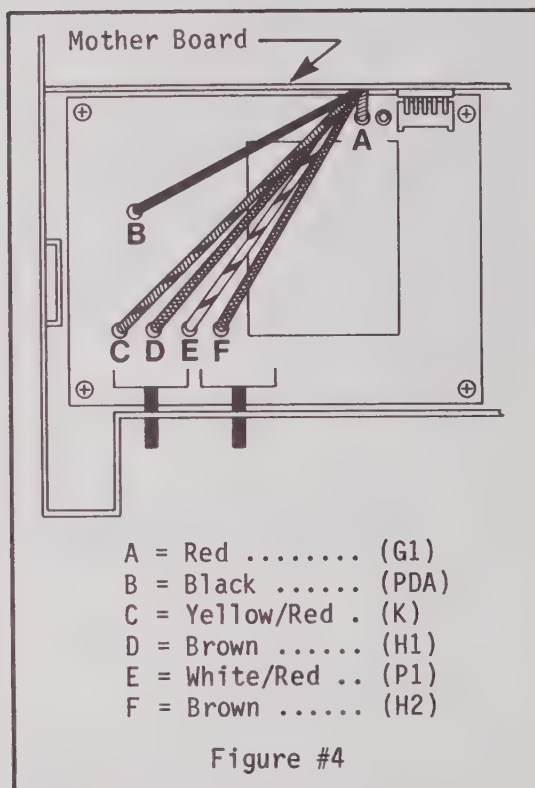
- #3. Install the Mother board (Figure #1).



- #4. Connect the six CRT connector wires to the High Voltage board (Figure #4).

WARNING: Install the CRT during the next step with care.

- #5. Slide the CRT into its shield and plug the high voltage anode wire onto the CRT (Figure #3).
- #6. Slide the CRT the rest of the way into the shield.
- #7. Plug in the CRT cable (Figure #5) to the rear of the CRT display.
- #8. Secure the high voltage anode wire to the wire holder on top of the CRT shield.
- #9. Connect the ground wire to the CRT shield (Figure #5).



INSTALLING THE HIGH VOLTAGE BOARD

This procedure installs the High Voltage board.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Install the High Voltage board and secure with a securing screw in each of its corners.
- #2. Install the Mother & Display Amp boards (page 9-7).

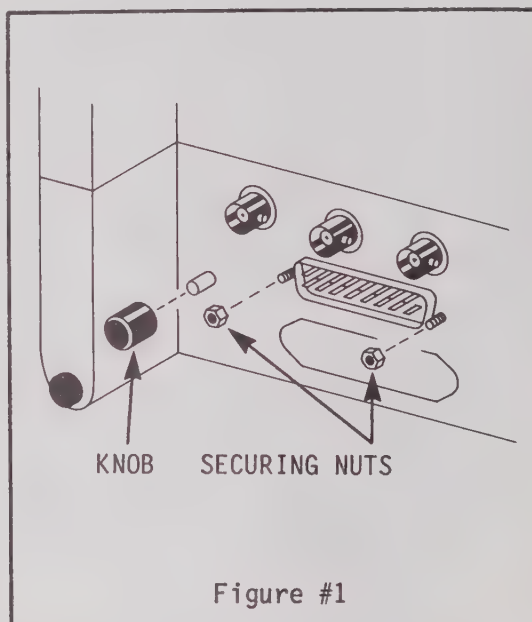
INSTALLING THE REAR PANEL/PEN POT BOARDS

This procedure installs the Rear Panel and Pen Pot boards.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Install the Rear Panel and Pen Pot boards assembly and secure with four securing screws.
- #2. Replace the two RS-232 connector securing nuts (Figure #1).
- #3. Replace the Pen Speed pot knob and secure (Figure #1).



INSTALLING THE EXTERNAL CONTROL BOARD

This procedure installs the External Control accessory board.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Plug in the External Control board to the Mother board (Figure #1).

(Not Available At This Time)

Figure #1

INSTALLING THE BUBBLE MEMORY HOLDER

This procedure installs the Bubble Memory holder accessory.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

CAUTION: The bubble memory is equipped with static sensitive components. Ground yourself properly before proceeding to guard against component damage.

PROCEDURE

- #1. Install and secure the Bubble Memory holder with four securing screws (Figure #1).
- #2. Install the Mother board (if it was removed) before continuing (page 9-7).
- #3. Reconnect the Bubble Memory ribbon cable to the Bubble Memory holder (Figure #1).

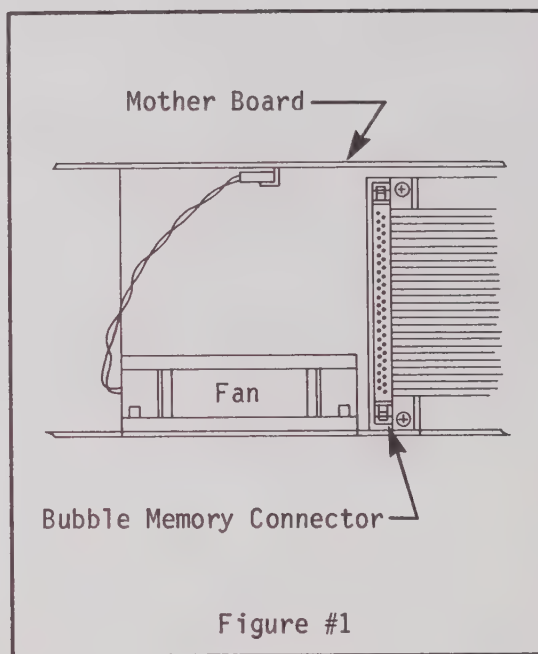


Figure #1

INSTALLING THE POWER SUPPLY

This procedure installs the Power Supply.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

- #1. Assemble the power supply shield, board, and bracket as illustrated in Figure #1).
- #2. Secure the assemblies with five securing screws (Figure #1).

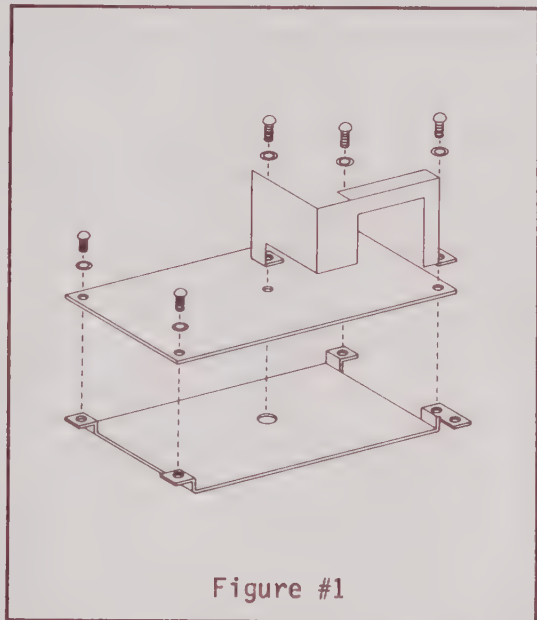
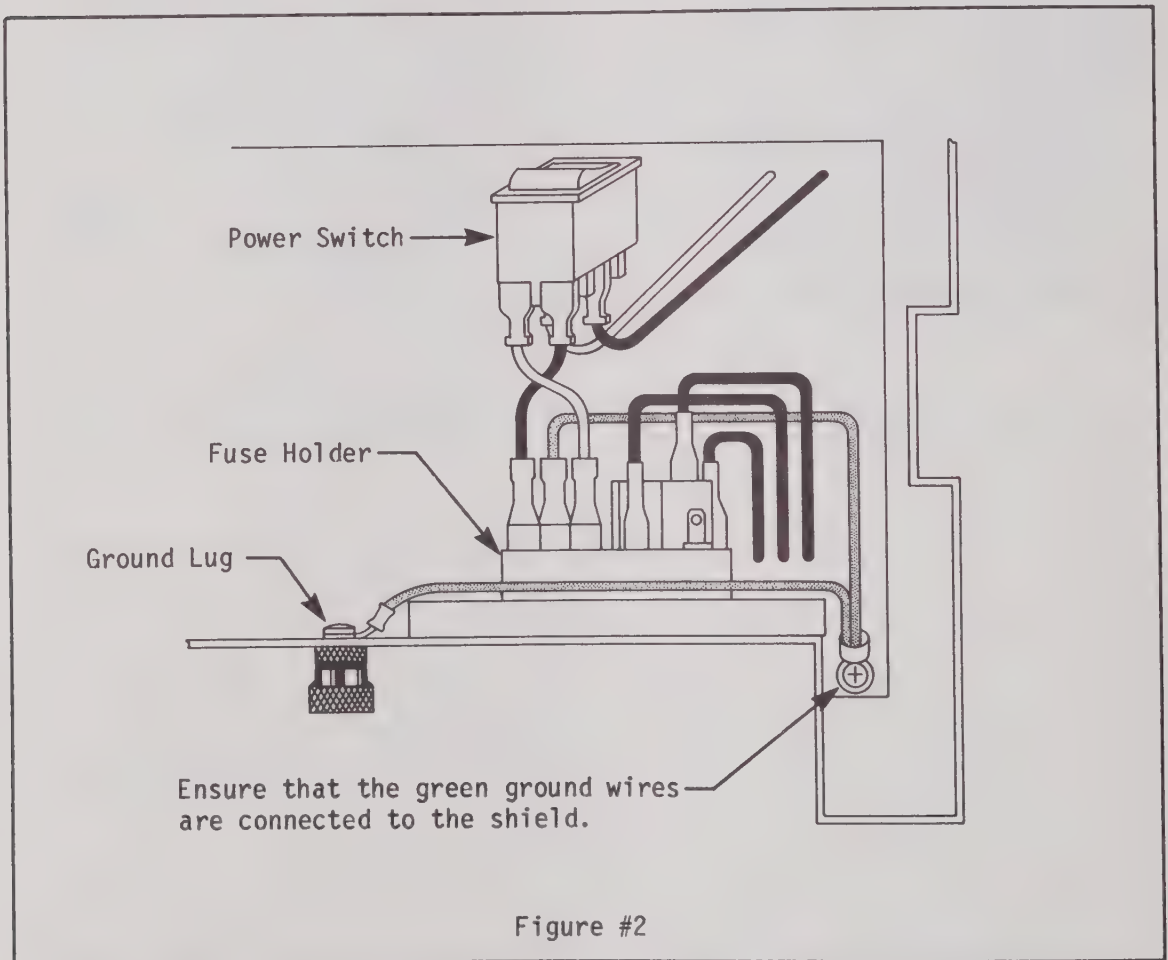


Figure #1

- #3. Mount the Grounding Lug and secure the green ground wire (Figure #2).
- #4. Plug in the six wires to the rear panel fuse holder (Figure #2).
- #5. Mount the Power ON/OFF switch to the top cover.



INSTALLING THE CRT DISPLAY

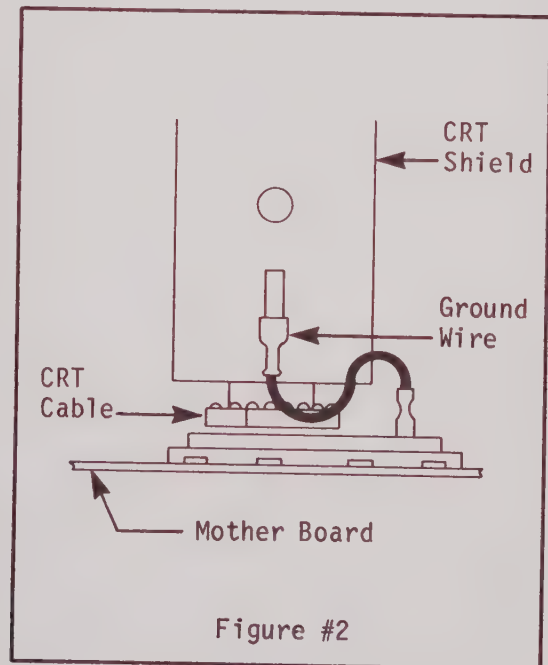
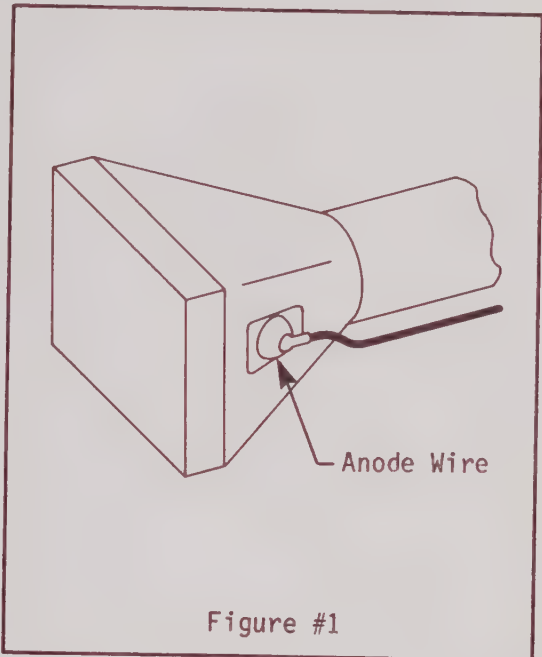
This procedure installs the CRT display.

CAUTION: High voltages exist within this instrument. Remove all power before proceeding.

PROCEDURE

WARNING: Perform this procedure with care to guard against personal injury or damage to the CRT.

- #1. Carefully slide the CRT into its shield and plug the high voltage anode wire into the CRT (Figure #1).
- #2. Plug the CRT connector unto the rear of the CRT (Figure #2).
- #3. Plug the CRT shield ground wire unto the CRT shield (Figure #2).



INTRODUCTION

WARNING: High voltages exist within the instrument. Safety standards set by your place of employment should be observed while servicing the instrument.

► **IMPORTANT:** Review the Caution Notes (Section 4) and each procedure in its entirety before proceeding with the actual service steps. If any questions or problems arise, contact:

Nicolet Instruments Corporation
Oscilloscope Division, Service Dept.
Madison, Wisconsin 53711
Telephone (608) 273-5010

If overseas, contact your local Nicolet representative.

Perform the alignment procedures in the order listed below.

PROCEDURE	PAGE
1 Voltage Checks	10-3
2 Reference Voltages	10-7
3 Clock Oscillator	10-11
4 Display Alignment	10-13
5 Balance Adjust	10-17
6 ADC Adjust	10-19
7 Voltage Calibration	10-23
8 Frequency Compensation	10-29
9 Input Capacitance	10-39
10 DC Zero Adjust	10-44

REQUIREMENTS

The instrument should be warmed up for at least 15 minutes with all covers in place before beginning.

TEST EQUIPMENT (Examples enclosed in parenthesis are typical.)

- Function generator: Sine, square, and triangle to 5 MHz, 100 mVpp to 20 Vpp (Wavetek 190)
- Digital voltmeter: $3\frac{1}{2}$ digit (Fluke 8060A)
- DC voltage standard: 5 digit, 400 mV - 11.1V min (Analogic AN3100)
- Frequency counter: Rated up through 20 MHz (Fluke 1912)
- Constant amplitude generator: 0.25 dB Flatness, 1MHz - 50MHz (Wavetek 1080)

TOOLS

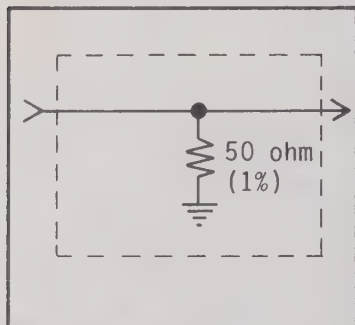
- Phillips screwdriver
- Nonmetallic, nonconductive alignment tool

WARNING: Use a nonmetallic, nonconductive alignment tool when making adjustments. Follow all safety standards set by your place of employment.

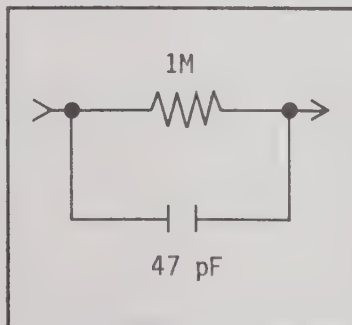
ATMOSPHERIC CONDITIONS (Room Ambient)

- Temperature: $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ($77^{\circ}\text{F} \pm 9^{\circ}\text{F}$)
- Humidity: 40%

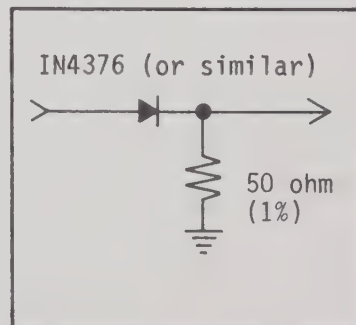
CIRCUITS



50 Ohm Terminator
Figure #1



RC Network
Figure #2



Diode Network
Figure #3

1.0.0. VOLTAGE CHECKS

1.1.0. TEST EQUIPMENT

- a. Digital Voltmeter (3½ digits)

1.2.0. SET-UP

1.2.1. General Controls

- a. Power ON
- b. Horizontal Expansion: xx
- c. Vertical Expansion: xx
- d. Autocenter: xx
- e. Display: xx
- f. Storage: xx
- g. Time Per Point: xx

1.2.2. Trigger Controls

- a. Trigger Mode: xx
- b. Trigger Slope: xx
- c. Trigger Coupling: xx
- d. Trigger Source: xx
- e. Pretrigger: xx

1.2.3. Channel A Controls

- a. On/Off: xx
- b. Save: xx
- c. DC Offset: xx
- d. Volts Full Scale: xx
- e. Input Coupling: xx

1.2.4. Channel B Controls

- a. On/Off: xx
- b. Save: xx
- c. DC Offset: xx
- d. Volts Full Scale: xx
- e. Input Coupling: xx

xx = Don't Care

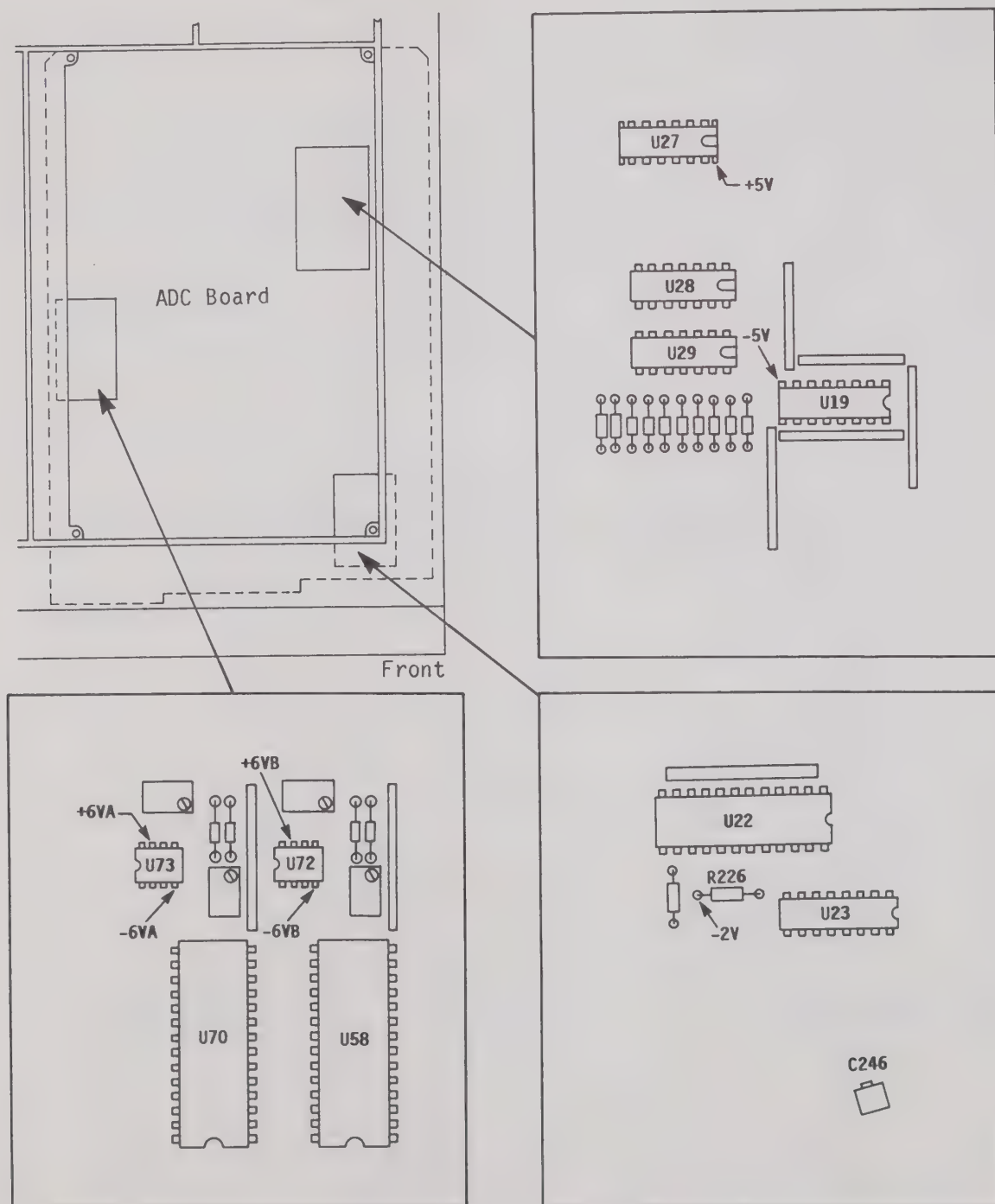


Figure 1-1

1.3.0. PROCEDURE

- 1.3.1. Lift the top cover of the 320 and remove the four securing screws that hold down the large metal cover to access the ADC board (Figure 1-2).

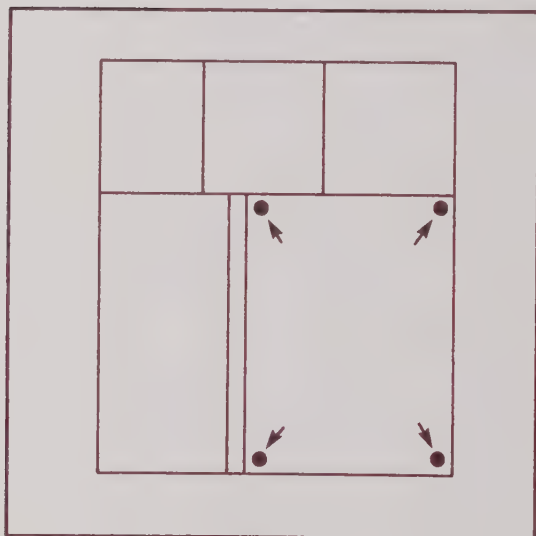


Figure 1-2

- 1.3.2. Using a DVM, measure the -5 volt test point on the ADC board. (Pin 8 of U19, Figure 1-1).

1.3.3.

SPECIFICATION
The DVM should read -4.70 to -4.80 volts. Adjust the -5 volt pot (Figure 1-3) only if the above spec is not met.

- 1.3.4. Using a DVM, measure the +5 volt test point on the ADC board. (Pin 16 of U27, Figure 1-1).

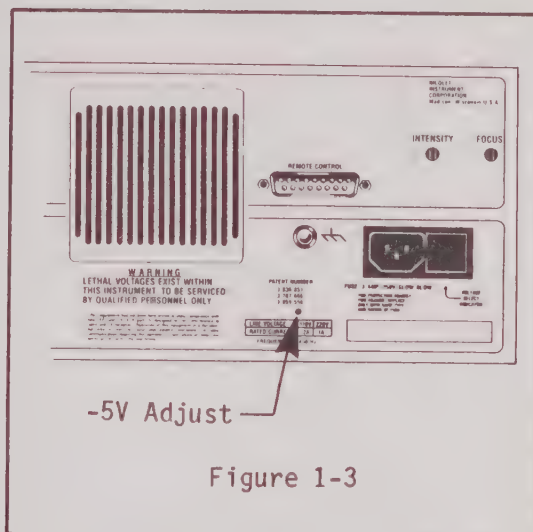


Figure 1-3

1.3.5.

SPECIFICATION
The DVM should read between +4.75 and +5.25 volts.

- 1.3.6. Measure the voltage at each test point in Table 1-1. See Figure 1-1 for test point locations. There are no adjustments.

TEST POINT	MEASURE AT -	THE DVM READING SHOULD RANGE -
+6VA	U73 Pin 7	+5.75V to +6.25V
-6VA	U73 Pin 4	-5.75V to -6.25V
+6VB	U72 Pin 7	+5.75V to +6.25V
-6VB	U72 Pin 4	-5.75V to -6.25V
-2V	R226	-1.8V to -2.2V

Table 1-1

2.0.0. REFERENCE VOLTAGE ADJUSTMENTS

2.1.0. TEST EQUIPMENT

- a. Digital Voltmeter, 3½ digits

2.2.0. SET-UP

2.2.1. General Controls

- a. Power: ON
- b. Horizontal Expansion: xx
- c. Vertical Expansion: xx
- d. Autocenter: xx
- e. Display: xx
- f. Storage: xx
- g. Time Per Point: xx

2.2.2. Trigger Controls

- a. Trigger Mode: xx
- b. Trigger Slope: xx
- c. Trigger Coupling: xx
- d. Pre-trigger: xx
- e. Trigger Source: xx

2.2.3. Channel A Controls

- a. On/Off: xx
- b. Volts Full Scale: xx
- c. Input Coupling: xx
- d. Save: xx
- e. DC Offset: xx

2.2.4. Channel B Controls

- a. On/Off: xx
- b. Volts Full Scale: xx
- c. Input coupling: xx
- d. Save: xx
- e. DC Offset: xx

xx = Don't Care

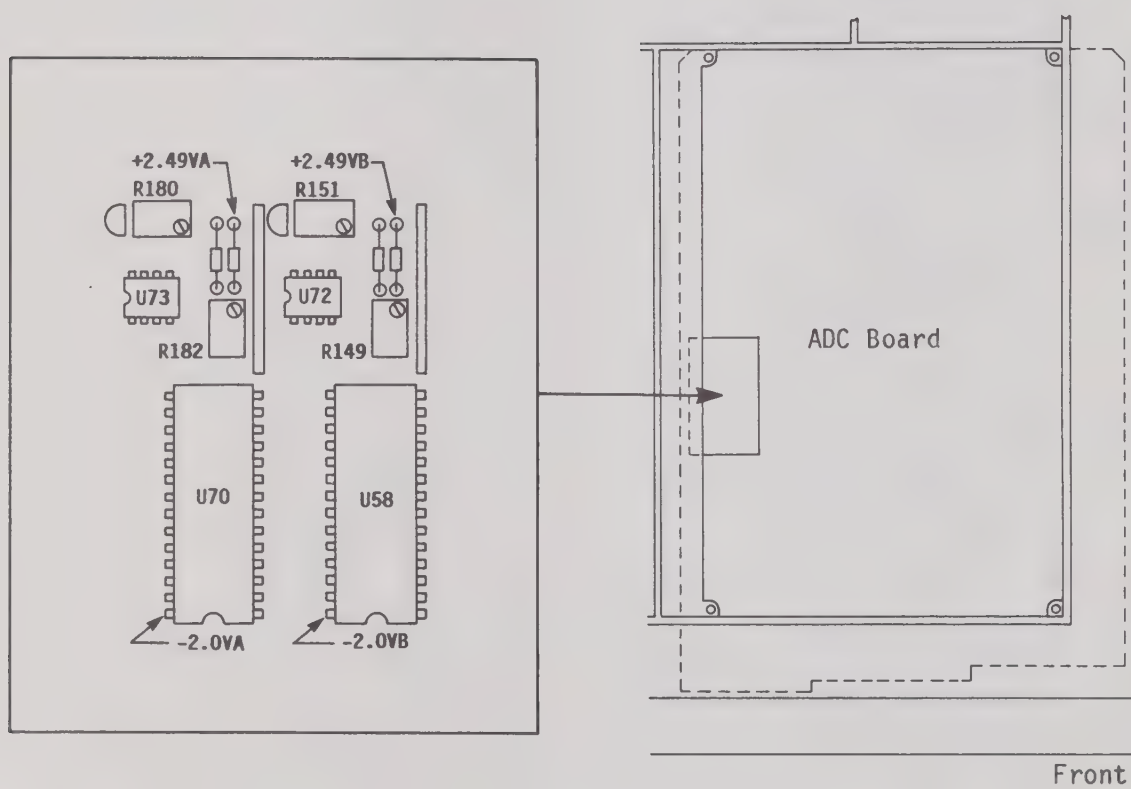


Figure 2-1

2.3.0. CHANNEL A ADJUST

2.3.1. Using a DVM, measure the voltage at the +2.49VA test point on the anode of CR36 (Figure 2-1).

2.3.2.

SPECIFICATION
If necessary, adjust R182 until the DVM reads +2.47V to +2.51V (Figure 2-1).

2.3.3. Using a DVM, measure the voltage at the -2.00VA test point (U70 - pin 28, Figure 2-1).

2.3.4.

SPECIFICATION
If necessary, adjust R180 until the DVM reads -1.98V to -2.02V (Figure 2-1).

2.4.0. CHANNEL B ADJUST

2.4.1. Using a DVM, measure the voltage at the +2.49VB test point on the anode of CR26 (Figure 2-1).

2.4.2.

SPECIFICATION
If necessary, adjust R149 until the DVM reads +2.47V to +2.51V (Figure 2-1).

2.4.3. Using a DVM, measure the voltage at the -2.00VB test point (U58 - pin 28, Figure 2-1).

2.4.4.

SPECIFICATION
If necessary, adjust R151 until the DVM reads -1.98 to -2.02V (Figure 2-1).

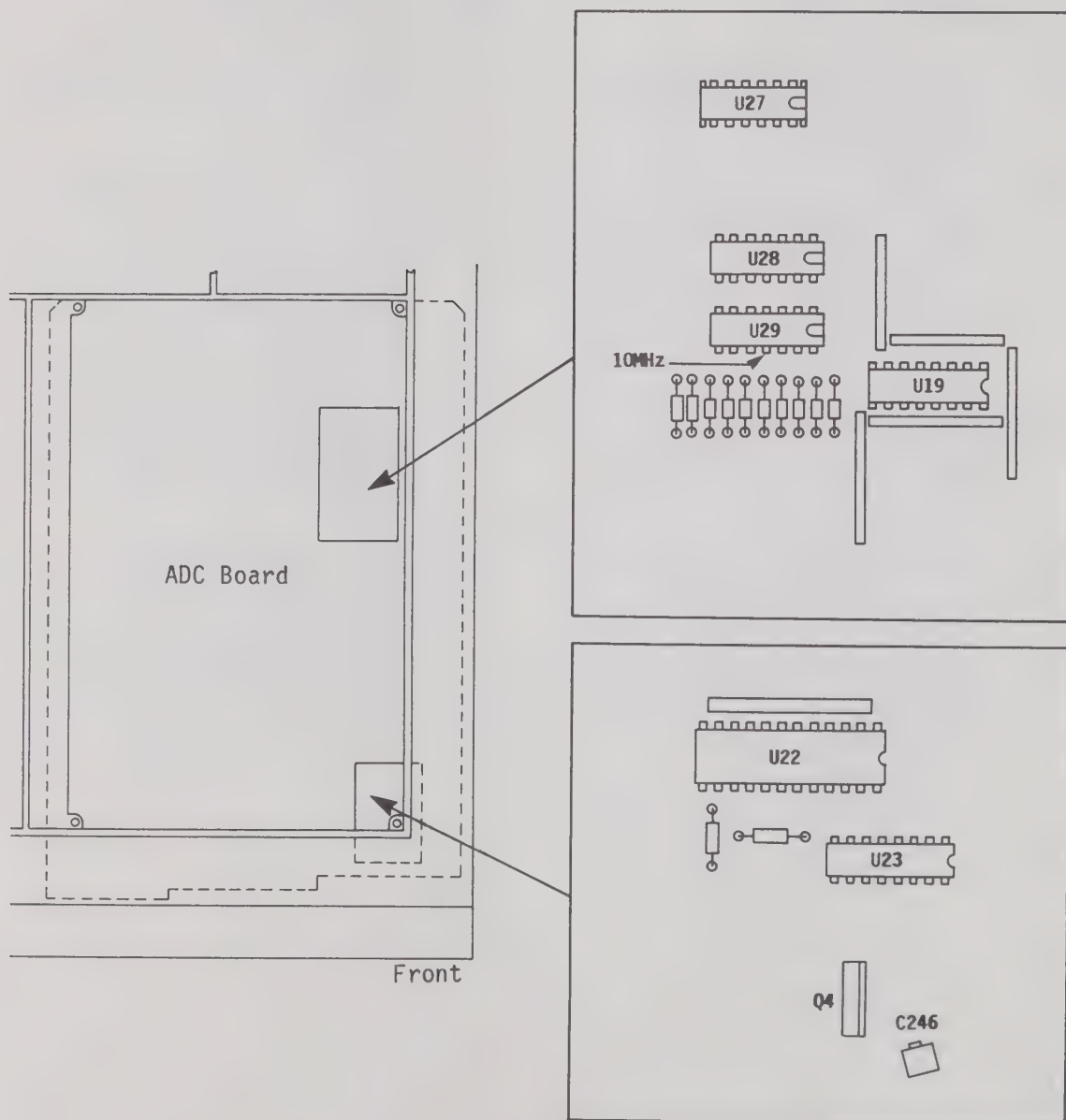


Figure 3-1

3.0.0. CLOCK OSCILLATOR ADJUST**3.1.0. TEST EQUIPMENT**

- a. Frequency Counter

3.2.0. SET-UP**3.2.1. General Controls**

- a. Power ON
- b. Horizontal Expansion: xx
- c. Vertical Expansion: xx
- d. Autocenter: xx
- e. Display: xx
- f. Storage: xx
- g. Time Per Point: xx

3.2.2. Trigger Controls

- a. Trigger Mode: xx
- b. Trigger Slope: xx
- c. Trigger Coupling: xx
- d. Trigger Source: xx
- e. Pre-trigger: xx

3.2.3. Channel A Controls

- a. On/Off xx
- b. Save xx
- c. DC Offset xx
- d. Volts Full Scale xx
- e. DC Offset xx
- f. Input Coupling xx

3.2.4. Channel B Controls

- a. On/Off xx
- b. Save xx
- c. DC Offset xx
- d. Volts Full Scale xx
- e. DC Offset xx
- f. Input coupling xx

3.3.0. PROCEDURE

NOTE: The scope should be at its operating temperature while performing this procedure.

- 3.3.1. Using a frequency counter, measure the frequency at the TTL-level, 10 MHz test point (U29, pin 11, Figure 3-1).

3.3.2.**SPECIFICATION**

If necessary, adjust C246 (Figure 3-1) until the counter reads 9.999 MHz to 10.001 MHz.

- 3.3.2. Turn the scope off.

- 3.3.3. After 10 seconds, turn the scope on again and verify that the frequency is still within specification and locked.

xx = Don't Care

4.0.0. DISPLAY ALIGNMENT

4.1.0. SET-UP

4.1.1. General Controls

- a. Power: ON
- b. Horizontal Expansion: OFF
- c. Vertical Expansion: OFF
- d. Autocenter: OFF
- e. Grid: ON
- f. Display: YT
- g. Time Per Point: 1 μ S
- h. Storage: HOLD LAST

4.1.2. Trigger Controls

- a. Trigger Mode: xx
- b. Trigger Slope: xx
- c. Trigger Coupling: xx
- d. Trigger Source: xx
- e. Pre-trigger: xx

4.1.3. Channel A Controls

- a. On/Off: ON
- b. Save: OFF
- c. Volts Full Scale: 1.5V
- d. Input Coupling: GND
- e. DC Offset: Centered

4.1.4. Channel B Controls

- a. On/Off: ON
- b. Save: OFF
- c. Volts Full Scale: 1.5V
- d. Input Coupling: GND
- e. DC Offset: Centered

xx = Don't Care

4.2.0. ACCESSING THE TRIM POTS

The trim pots are located below the left rear compartment of the instrument's equipment tray (Figure 4-1). They are accessed by lifting the compartment pad.

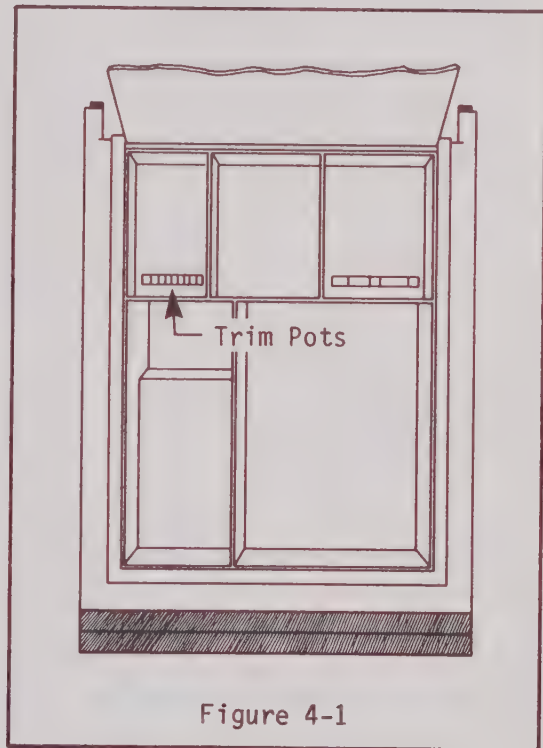
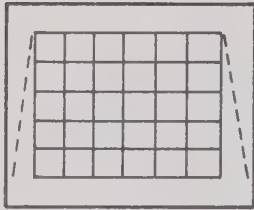
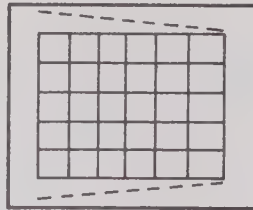


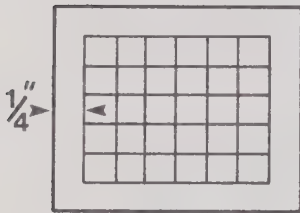
Figure 4-1



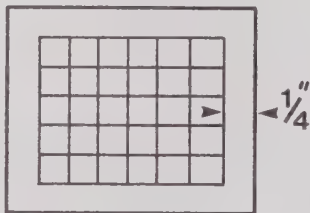
X-Rotation
Figure 4-2



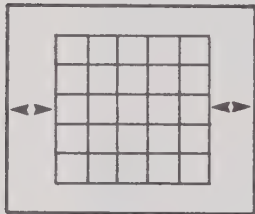
Y-Rotation
Figure 4-3



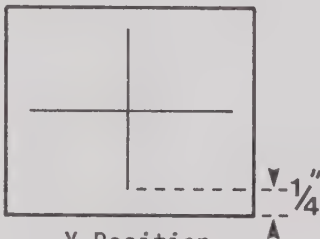
YTX Position
Figure 4-4



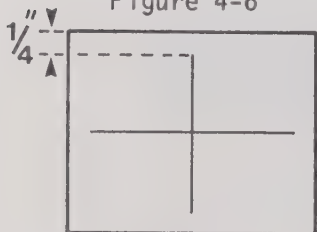
X-Gain
Figure 4-5



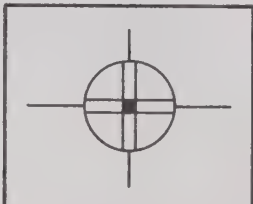
XYX Position
Figure 4-6



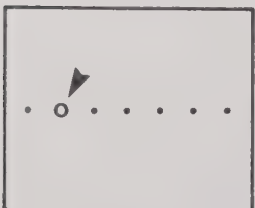
Y-Position
Figure 4-7



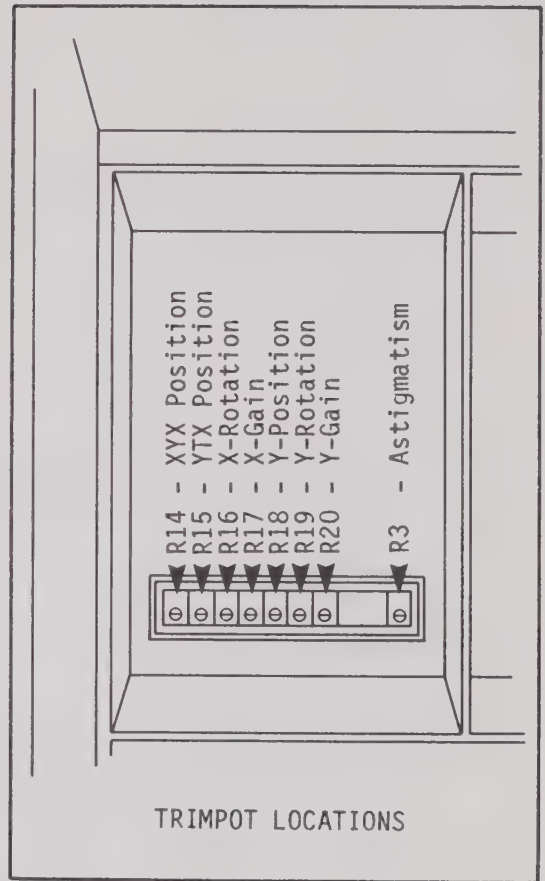
Y-Gain
Figure 4-8



Astigmatism
Figure 4-9



Focus
Figure 4-10



4.3.0. ALIGNMENT PROCEDURE

► **IMPORTANT:** Align the display only when necessary and in the sequence listed below.

WARNING: Hazardous voltages exist within the instrument, use care and a nonconductive adjustment tool only. Follow all safety rules set by your place of employment.

X-ROTATION: (Figure 4-2)

Adjust R16 until the vertical grid lines are parallel with the side of the screen.

Y-ROTATION: (Figure 4-3)

Adjust R19 until the horizontal grid lines are parallel with the top of the screen.

YTX POSITION: (Figure 4-4)

Adjust R15 until the left edge of the grid is approximately 1/4" from the left edge of the screen.

X-GAIN: (Figure 4-5)

Adjust R17 until the right side of the grid is 1/4" from the right side of the screen.

XYX POSITION: (Figure 4-6)

Select the XY display mode and adjust R14 until the grid is centered horizontally on the screen.

Y-POSITION: (Figure 4-7)

Switch GRID off, select the YT display mode, and position the vertical cursor to the approximate center of the screen. Adjust R18 until the bottom of the vertical cursor is 1/4" from the bottom of the screen.

Y-GAIN: (Figure 4-8)

Adjust R20 until the top edge of the Vertical cursor is 1/4" from the top of the screen.

ASTIGMATISM: (Figure 4-9)

Position the horizontal cursor such that it does not lie on a trace, and is still visible near the center of the screen.

Using the rear panel FOCUS control, slightly unfocus the display and adjust R3 until the two cursors have the same thickness.

FOCUS: (Figure 4-10)

Expand horizontally (◀▶) until individual data points are visible.

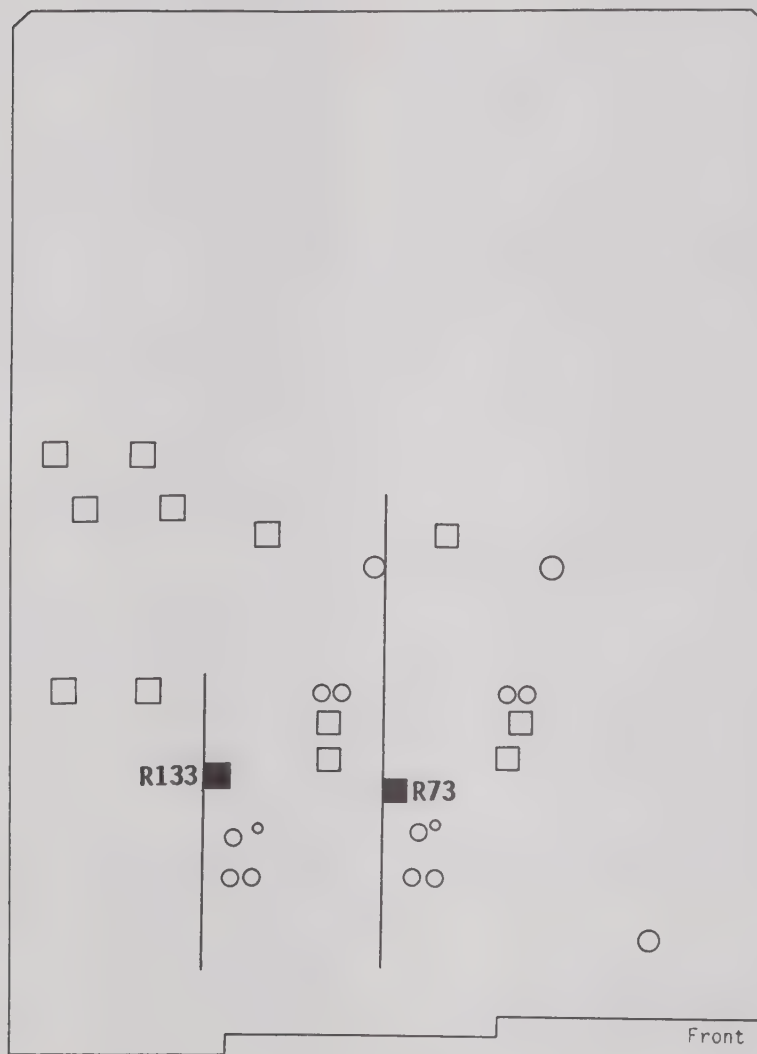
Locate a data point approximately 25% of the distance from screen left and adjust the rear panel FOCUS control until the data point is in focus (round and of minimum size).

Turn horizontal expansion off.

INTENSITY

Adjust the rear panel INTENSITY control as required. Note that too high a setting adversely affects focus.

Reinstall the cover pad over the trimpots.



ADC Board
Figure 5-1

5.0.0. BALANCE ADJUST

5.1.0. SET-UP

5.1.1. General Controls

- a. Power: ON
- b. Hor. Expansion: OFF
- c. Vert. Expansion: OFF
- d. Autocenter: OFF
- e. Display: YT
- f. Storage: LIVE
- g. Time Per Point: 100 nS

5.1.2. Trigger Controls

- a. Trigger Mode: AUTO
- b. Trigger Slope: +
- c. Trigger Coupling: DC
- d. Pre-trigger: ZERO
- e. Trigger Source: EXT

5.1.3. Channel A Controls

- a. On/Off: ON
- b. Volts Full Scale: 1.5V
- c. Input Coupling: GND
- d. Save: OFF
- e. DC Offset: Screen Center

5.1.4. Channel B Controls

- a. On/Off: OFF
- b. Volts Full Scale: 1.5V
- c. Input Coupling: GND
- d. Save: OFF
- e. DC Offset: Screen Center

5.2.0. CHANNEL A ADJUST

► **IMPORTANT:** The scope must have been running at least 1/2 hour before proceeding with the Balance adjustment. Leave the top cover closed except when actually making an adjustment.

5.2.1. Turn the GRID mode on and use the grid as a reference for the following steps.

5.2.2. While observing the trace for a vertical shift, switch the channel A Volts Full Scale switch between the 600mV and 1.5V ranges.

5.2.3.

SPECIFICATION

If the trace shifts more than 1/4 division, adjust pot R133 (Figure 5-1) until the trace remains stationary while switching ranges. Use Vertical Expansion if necessary.

5.3.0. CHANNEL B ADJUST

5.3.1. Channel B on, channel A off.

5.3.2. While observing the trace for a vertical shift, switch the channel B Volts Full Scale switch between the 600mV and 1.5V ranges.

5.3.3.

SPECIFICATION

If the trace shifts more than 1/4 division, adjust pot R73 (Figure 5-1) until the trace remains stationary while switching ranges. Use Vertical Expansion if necessary.

6.0.0. ADC ADJUST

6.1.0. TEST EQUIPMENT

- a. Function generator
- b. 50 ohm terminator (Figure #1, page 10-2)

6.2.0. SET-UP

6.2.1. General Controls

- a. Horizontal Expansion: OFF
- b. Vertical Expansion: OFF
- c. Autocenter: OFF
- d. Display: YT
- e. Grid: OFF
- f. Storage: LIVE
- g. Time Per Point: 100 nS

6.2.2. TRIGGER CONTROLS

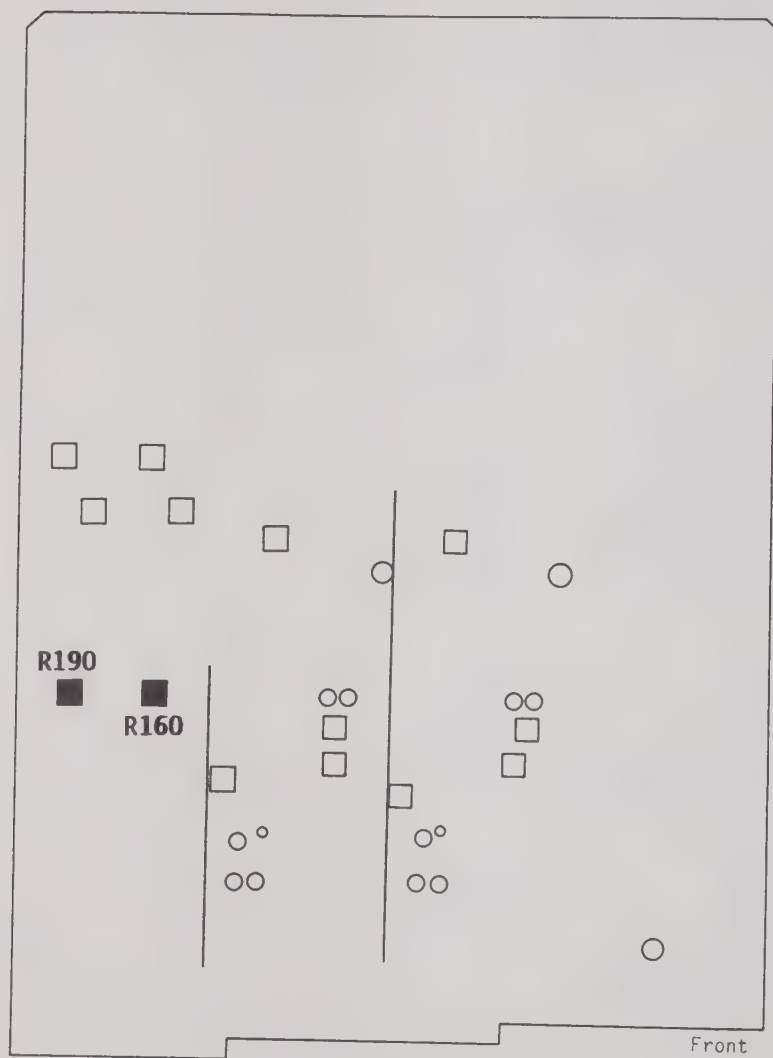
- a. Trigger Mode: AUTO
- b. Trigger Slope: +
- c. Trigger Coupling: DC
- d. Trigger Source: EXT
- e. Pre-trigger: ZERO

6.2.3. CHANNEL A

- a. On/Off: ON
- b. Save: OFF
- c. DC Offset: CENTER
- d. Volts Full Scale: 1.5 V
- e. Input Coupling: DC

6.2.4. CHANNEL B

- a. On/Off: OFF
 - b. Save: OFF
 - c. DC Offset: CENTER
 - d. Volts Full Scale: 1.5 V
 - e. Input Coupling: DC
-



ADC Board
Figure 6-1

6.3.0. CHANNEL A ADJUST

- 6.3.1. Connect the generator's sync output to the EXT TRIG BNC and adjust the trigger LEVEL control for a stable TRG'D LED indication.
- 6.3.2. Using a 50 ohm terminator (Figure #1, page 10-2), input a 5 MHz sine wave to the channel A input BNC and adjust the generator amplitude for a 3/4 screen output.
- 6.3.3. Adjust the generator output frequency very slightly until several cycles are displayed on screen. The signal observed is a low frequency alias of the input frequency and may appear to be unstable.

6.3.4.

SPECIFICATION

If any "glitches" or gaps are observed on the waveform, adjust pot R190 for the best sine wave (Figure 6-1).

- 6.3.5. Apply a 1200 Hz triangle wave to the channel A input BNC.

6.3.6.

SPECIFICATION

Check for any "glitches" or gaps on the diagonal line. (No adjustment.)

6.4.0. CHANNEL B ADJUST

- 6.4.1. Channel B on, channel A off.
- 6.4.2. Using a 50 ohm terminator (Figure #1, page 10-2), input a 5 MHz sine wave to the channel B input BNC and adjust the generator amplitude for a 3/4 screen output.
- 6.4.3. Adjust the generator output frequency very slightly until several cycles are displayed on screen. The signal observed is a low frequency alias of the input frequency and may appear to be unstable.

6.4.4.

SPECIFICATION

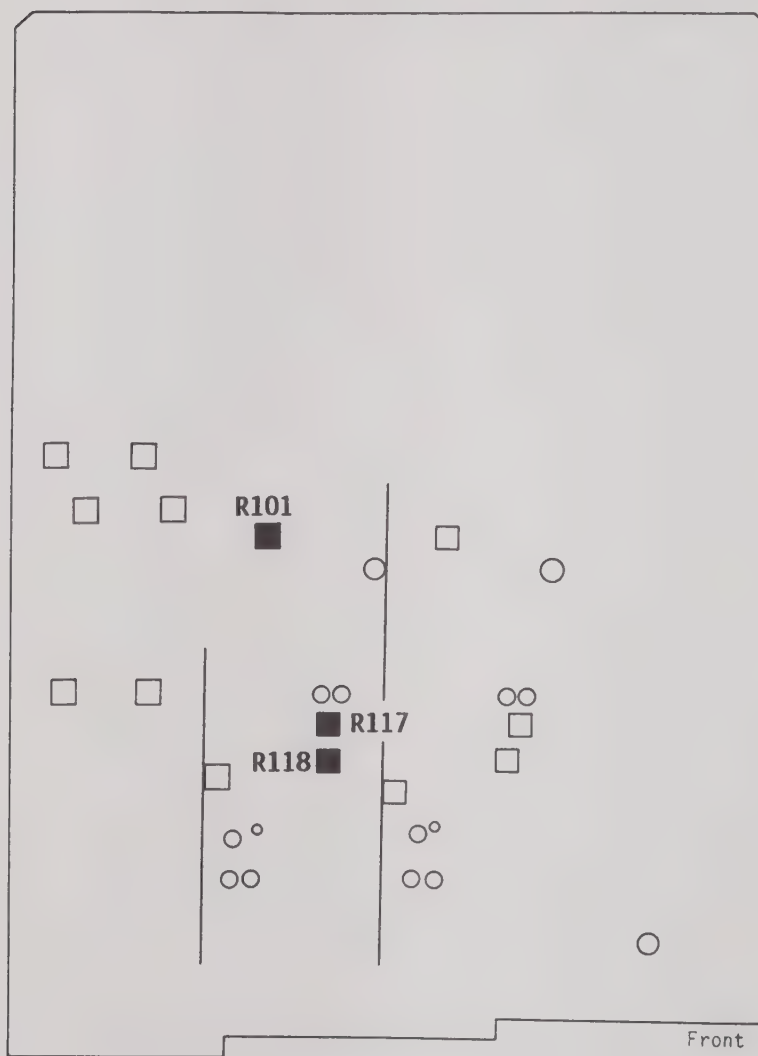
If any "glitches" or gaps are observed on the waveform, adjust pot R160 for the best sine wave (Figure 6-1).

- 6.4.5. Apply a 1200 Hz triangle wave to the channel B input BNC.

6.4.6.

SPECIFICATION

Check for any "glitches" or gaps on the diagonal line. (No adjustment.)



ADC Board
Figure 7-1

7.3.0. CHANNEL A ADJUST

7.3.1. Using a precision DC voltage source, input -1126 mV to the channel A input BNC.

7.3.2. Press HOLD NEXT, then reverse the polarity of the voltage source while the scope is still sweeping. Both a negative and positive segment must be captured.

7.3.3. Vertical Expansion: Press button five times.

7.3.4. Using the left/right Cursor buttons, position the crosshair to the negative voltage level containing the most data points.

7.3.5. Press the Numerics Reset button, resetting the time and voltage numerics to 00.

7.3.6. Using the left/right Cursor buttons, move the crosshair to the positive voltage level containing the most data points.

7.3.7.

SPECIFICATION

The voltage value displayed by the voltage numerics should be within the values listed in Table 7-1.

If the voltage reading is not within spec's, adjust the corresponding pot.

7.3.8. Vertical Expansion: OFF

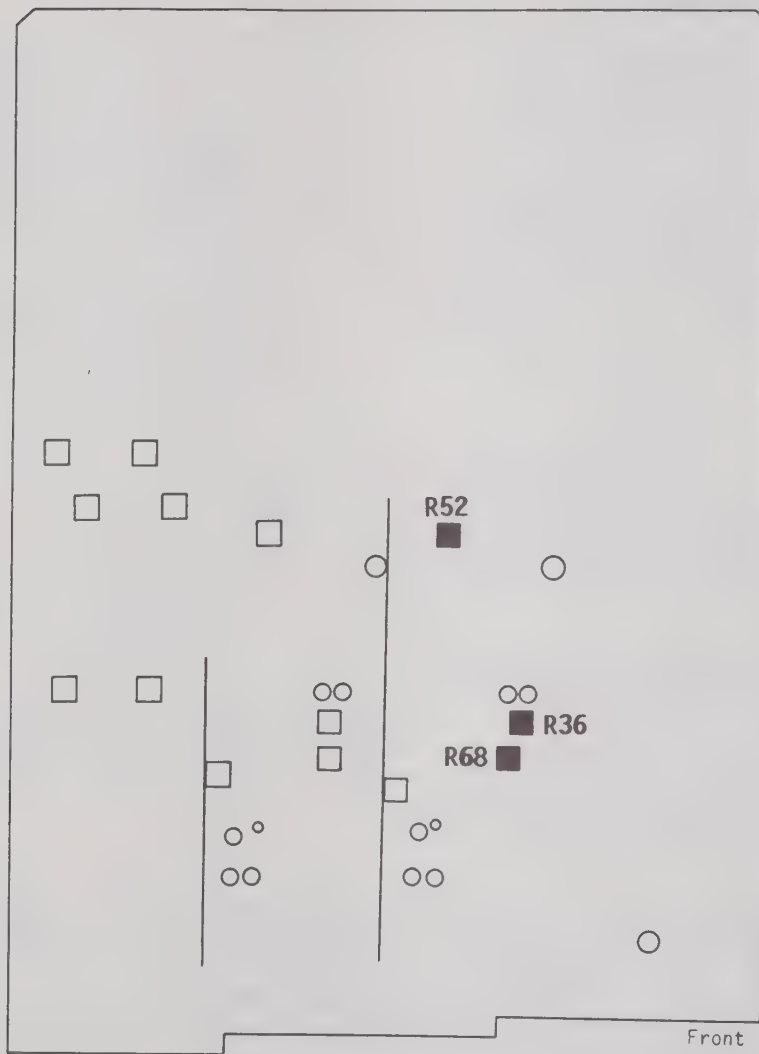
7.3.9. Numerics Reset: OFF

7.3.10. If necessary, repeat steps 7.3.2 - 7.3.9 until the voltage specification in Table 7-1 is met.

7.3.11. Repeat steps 7.3.1 through 7.3.10 for the next Volts Full Scale range in Table 7-1 until channel A is completed.

VOLTS FULL SCALE	INPUT VOLTAGE	(Tolerance = $\pm 1\%$ Full Scale)			CHANNEL A POTS (See Figure 7-1)
		MINIMUM	NOMINAL	MAXIMUM	
1.5 V	± 1126 mV	2220	2252.8	2285	R101 (incr. = cw)
3 V	± 2252 mV	4440	4505.6	4570	R118 (incr. = ccw)
6 V	± 4504 mV	8880	9011.2	9140	R117 (incr. = ccw)
600 mV	± 450.4 mV	888.0	901.12	914.0	No Adjustment
15 V	± 11.01 V	21.69	22.016	22.34	No Adjustment

Table 7-1



ADC Board
Figure 7-2

7.4.0. CHANNEL B ADJUST

7.4.1. Channel B on, channel A off.

7.4.2. Using a precision DC voltage source, input -1126 mV to the channel B input BNC.

7.4.3. Press HOLD NEXT, then reverse the polarity of the voltage source while the scope is still sweeping. Both a negative and positive segment must be captured.

7.4.4. Vertical Expansion: Press button five times.

7.4.5. Using the left/right Cursor buttons, position the crosshair to the negative voltage level containing the most data points.

7.4.6. Press the Numerics Reset button, resetting the time and voltage numerics to 00.

7.4.7. Using the left/right Cursor buttons, move the crosshair to the positive voltage level containing the most data points.

7.4.8.

SPECIFICATION

The voltage value displayed by the voltage numerics should be within the values listed in Table 7-2.

If the voltage reading is not within spec's, adjust the corresponding pot.

7.4.9. Vertical Expansion: OFF

7.4.10. Numerics Reset: OFF

7.4.11. If necessary, repeat steps 7.4.2 - 7.4.10 until the voltage specification in Table 7-2 is met.

7.4.12. Repeat steps 7.4.2 through 7.4.11 for the next Volts Full Scale range in Table 7-2 until channel B is completed.

VOLTS FULL SCALE	INPUT VOLTAGE	(Tolerance = $\pm 1\%$ Full Scale)			CHANNEL B POTS (See Figure 7-2)
		MINIMUM	NOMINAL	MAXIMUM	
1.5 V	± 1126 mV	2220	2252.8	2285	R52 (incr. = cw)
3 V	± 2252 mV	4440	4505.6	4570	R68 (incr. = ccw)
6 V	± 4504 mV	8880	9011.2	9140	R36 (incr. = ccw)
600 mV	± 450.4 mV	888.0	901.12	914.0	No Adjustment
15 V	± 11.01 V	21.69	22.016	22.34	No Adjustment

Table 7-2

8.0.0. FREQUENCY COMPENSATION

8.1.0. TEST EQUIPMENT

- a. RF generator
- b. Function generator
- c. 50 ohm terminator (Figure #1, page 10-2)
- d. Diode network (Figure #3, page 10-2)

8.2.0. SET-UP

8.2.1. General Controls

- a. Power: ON
- b. Horizontal Expansion: OFF
- c. Vertical Expansion: OFF
- d. Autocenter: ON
- e. Display: YT
- f. Grid: ON
- g. Storage: LIVE
- h. Time Per Point: 100 nS

8.2.2. Trigger Controls

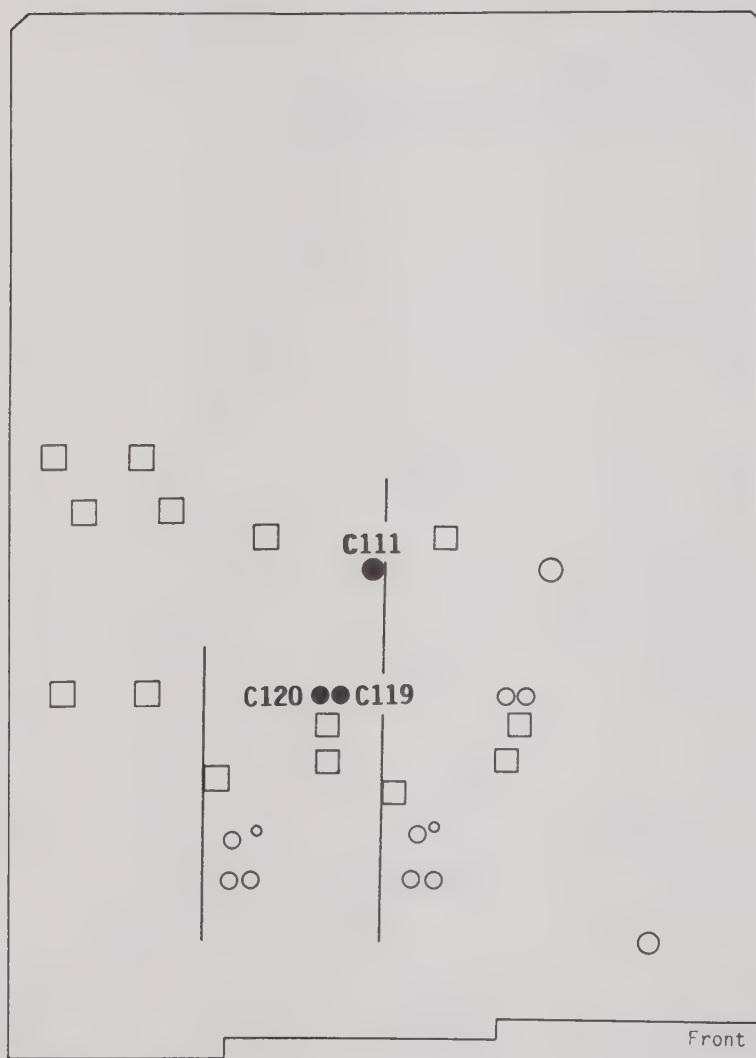
- a. Trigger Mode: AUTO
- b. Trigger Slope: +
- c. Trigger Coupling: DC
- d. Trigger Source: EXT
- e. Pre-trigger: ZERO

8.2.3. Channel A Controls

- a. On/Off: ON
- b. Save: OFF
- c. Volts Full Scale: 150 mV
- d. Input Coupling: DC
- e. DC Offset: Screen Center

8.2.4. Channel B Controls

- a. On/Off: OFF
 - b. Save: OFF
 - c. Volts Full Scale: 150 mV
 - d. Input Coupling: DC
 - e. DC Offset: Screen Center
-



ADC Board
Figure 8-1

**8.3.0. CHANNEL A COMPENSATION CHECK
(150mV, 300mV, & 600mV Ranges)**

8.3.1. Using a 50 ohm terminator (Figure #1, page 10-2) input a 1 MHz sine wave from the RF generator to channel A. Adjust the generator amplitude to exactly six grid divisions (approximately -9 dB).

8.3.2. Change the generator frequency to 15 MHz.

8.3.3.

SPECIFICATION

If the 15 MHz amplitude is not between 5.75 and 6.25 divisions, adjust C111 (Figure 8-1) for exactly six divisions.

8.3.4. Change the generator frequency to 25 MHz.

8.3.5.

SPECIFICATION

The 25 MHz amplitude must be at least 4.25 divisions. There is no adjustment.

8.3.6. Volts Full Scale: 300 mV

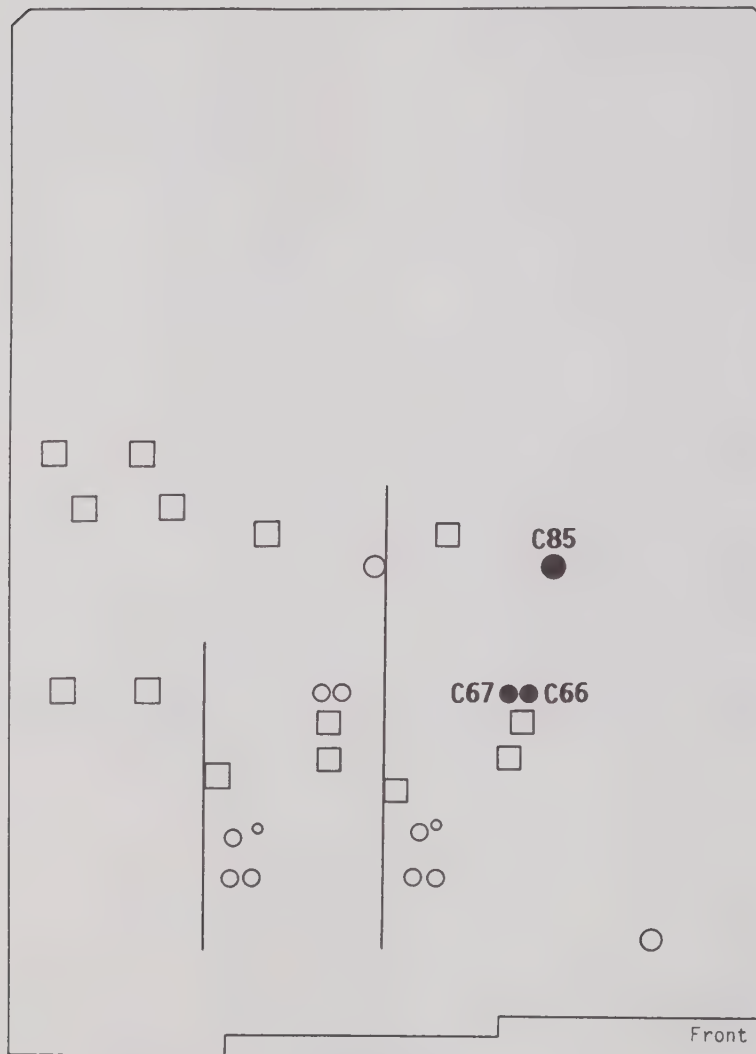
8.3.7. Increase the generator output to approximately -3 dB.

8.3.8. Repeat steps 8.3.1 through 8.3.5. If necessary, adjust C119 (Figure 8-1) in step 8.3.3.

8.3.9. Volts Full Scale: 600 mV

8.3.10. Increase the generator output to approximately +3 dB.

8.3.11. Repeat steps 8.3.1 through 8.3.5. If necessary, adjust C120 (Figure 8-1) in step 8.3.3.



ADC Board
Figure 8-2

**8.4.0. CHANNEL B COMPENSATION CHECK
(150mV, 300mV, & 600mV Ranges)**

8.4.1. Channel B on, channel A off.

8.4.2. Using a 50 ohm terminator (Figure #1, page 10-2) input a 1 MHz sine wave from the RF generator to channel B. Adjust the generator amplitude to exactly six grid divisions (approximately -9 dB).

8.4.3. Change the generator frequency to 15 MHz.

8.4.4.

SPECIFICATION

If the 15 MHz amplitude is not between 5.75 and 6.25 divisions, adjust C85 (Figure 8-2) for exactly six divisions.

8.4.5. Change the generator frequency to 25 MHz.

8.4.6.

SPECIFICATION

The 25 MHz amplitude must be at least 4.25% divisions. There is no adjustment.

8.4.7. Volts Full Scale: 300 mV

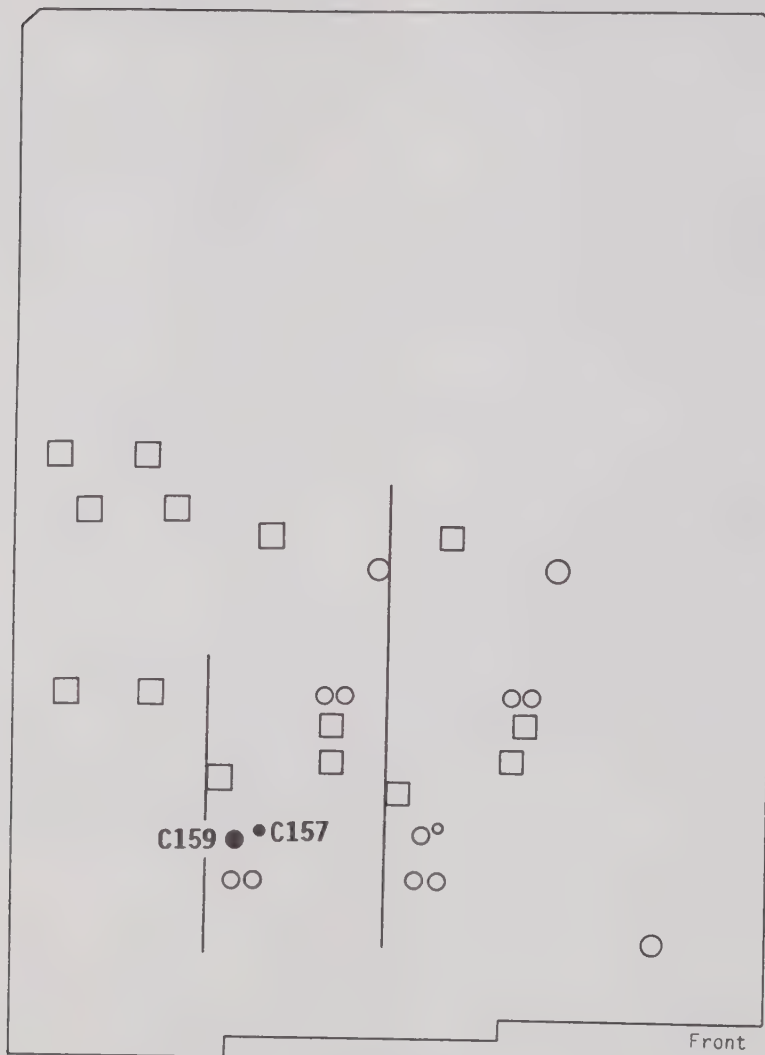
8.4.8. Increase the generator output to approximately -3 dB.

8.4.9. Repeat steps 8.4.2 through 8.4.6. If necessary, adjust C66 (Figure 8-2) in step 8.4.4.

8.4.10. Volts Full Scale: 600 mV

8.4.11. Increase the generator output to approximately +3 dB.

8.4.12. Repeat steps 8.4.2 through 8.4.6. If necessary, adjust C67 (Figure 8-2) in step 8.4.4.



ADC Board
Figure 8-3

8.5.0. CHANNEL A 1.5V & 15V COMPENSATION

8.5.1. Volts Full Scale: 1.5V

8.5.2. Turn the grid display off.

8.5.3. Connect the function generator's sync output to the EXT TRIG BNC and adjust the trigger LEVEL control for a stable trigger.

8.5.4. Input a 10 kHz square wave to the channel A input BNC via a diode network (Figure #2, page 10-2). Adjust the generator output amplitude for a signal from zero to near-positive full scale.

8.5.5. Using the left/right CURSOR buttons, position the cross-hair over the bottom of the square wave.

8.5.6. Tap the Horizontal Expansion button four times.

8.5.7. Tap the Vertical Expansion button twice.

8.5.8.

SPECIFICATION
If the bottom of the waveform is not flat, adjust C159 (Figure 8-3) for the best square wave.

8.5.9. Volts Full Scale: 15V

8.5.10. Increase the generator amplitude for a signal from zero to near-positive full scale.

8.5.11.

SPECIFICATION
If the bottom of the waveform is not flat, adjust C157 (Figure 8-3) for the best square wave.

8.5.12. Turn Horizontal and Vertical Expansion off.

8.5.13. Disconnect the function generator.

8.5.14. Volts Full Scale: 1.5V

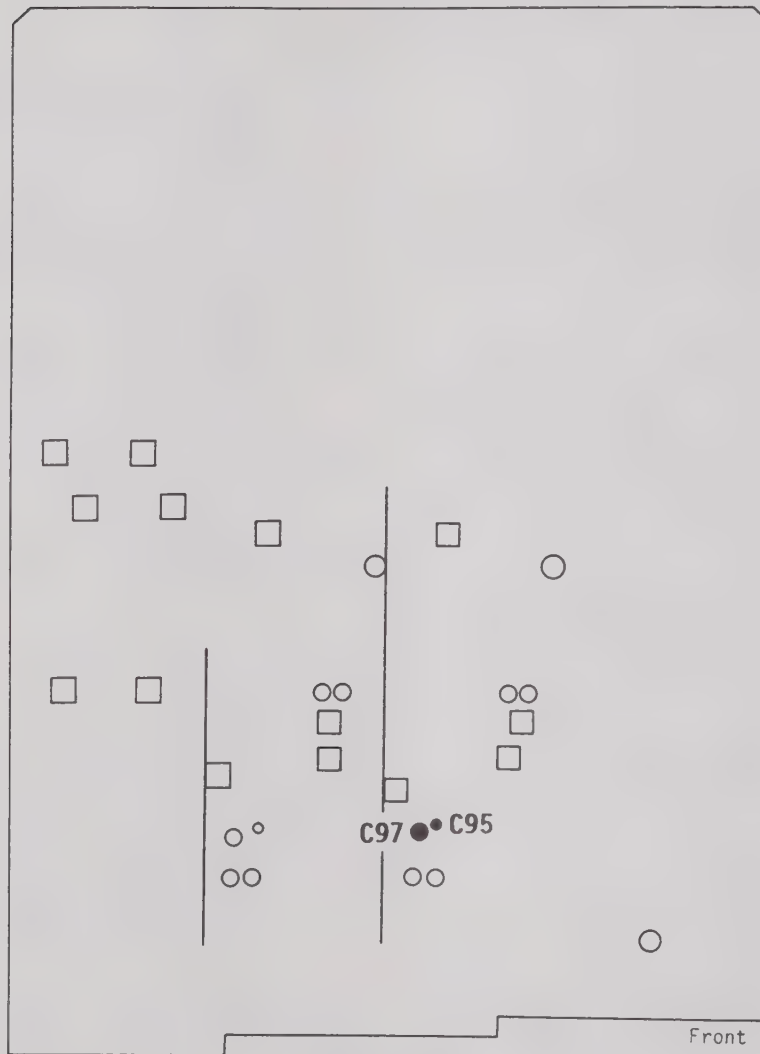
8.5.15. Turn the grid display on.

8.5.16. Using a 50 ohm terminator (Figure #1, page 10-2) input a 1 MHz sine wave from the RF generator to channel A. Adjust the generator amplitude to exactly six grid divisions (approximately +11 dB).

8.5.17. Change the generator frequency to 25 MHz.

8.5.18.

SPECIFICATION
The 25 MHz amplitude must be at least 4.25 divisions. There is no adjustment.



ADC Board
Figure 8-4

8.6.0. CHANNEL B 1.5V & 15V COMPENSATION

8.6.1. Channel B on, channel A off.

8.6.2. Volts Full Scale: 1.5V

8.6.3. Turn the grid display off.

8.6.4. Connect the generator's sync output to the EXT TRIG BNC and adjust the trigger LEVEL control for a stable trigger.

8.6.5. Input a 10 kHz square wave to the channel B input BNC via a diode network (Figure 8-4). Adjust the generator output amplitude for a signal from zero to near-positive full scale.

8.6.6. Using the left/right CURSOR buttons, position the cross-hair over the bottom of the square wave.

8.6.7. Tap the Horizontal Expansion button four times.

8.6.8. Tap the Vertical Expansion button twice.

8.6.9.

SPECIFICATION

If the bottom of the waveform is not flat, adjust C97 (Figure 8-4) for the best square wave.

8.6.10. Volts Full Scale: 15V

8.6.11. Increase the generator amplitude for a signal from zero to near-positive full scale.

8.6.12.

SPECIFICATION

If the bottom of the waveform is not flat, adjust C95 (Figure 8-4) for the best square wave.

8.6.13. Turn Horizontal and Vertical Expansion off.

8.6.14. Disconnect the function generator.

8.6.15. Volts Full Scale: 1.5V

8.6.16. Turn the grid display on.

8.6.17. Using a 50 ohm terminator (Figure #1, page 10-2) input a 1 MHz sine wave from the RF generator to channel B. Adjust the generator amplitude to exactly six grid divisions (approximately +11 dB).

8.6.18. Change the generator frequency to 25 MHz.

8.6.19.

SPECIFICATION

The 25 MHz amplitude must be at least 4.25 divisions. There is no adjustment.

9.0.0. INPUT CAPACITANCE ADJUST

9.1.0. TEST EQUIPMENT

- a. Function generator
- b. RC Network (Figure #2, page 10-2)

9.2.0. SET-UP**9.2.1. General Controls**

- a. Power: ON
- b. Horizontal Expansion: OFF
- c. Vertical Expansion: OFF
- d. Autocenter: OFF
- e. Display: YT
- f. Storage: LIVE
- g. Time Per Point: 100 nS

9.2.2. Trigger Controls

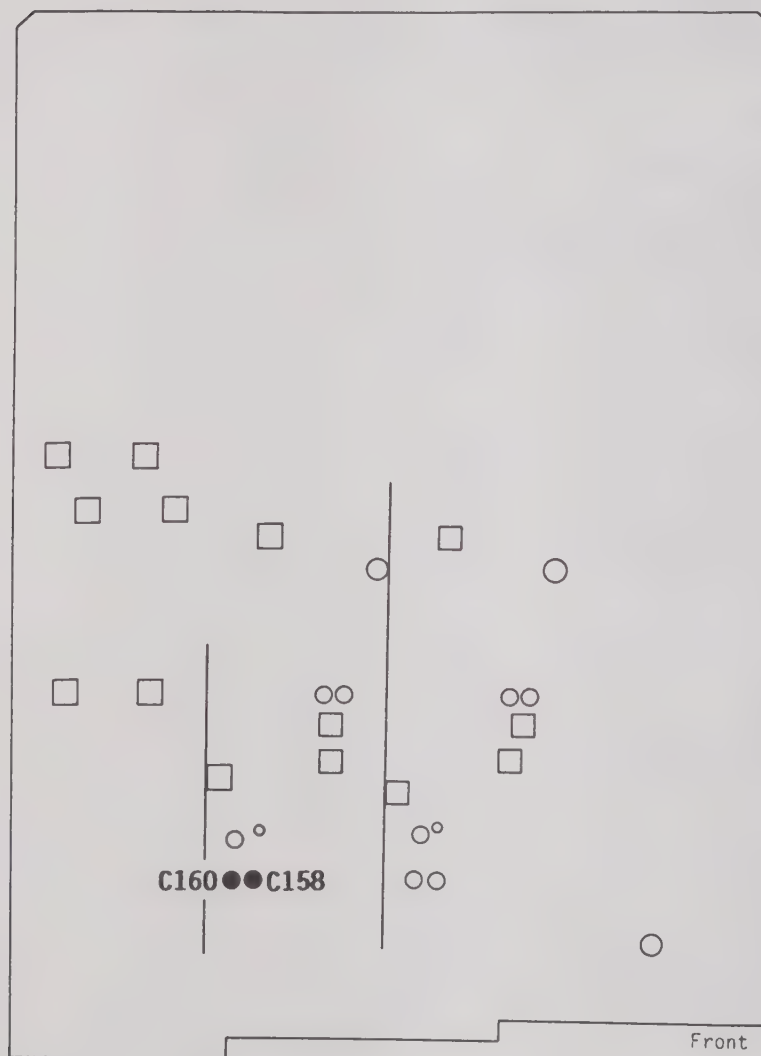
- a. Trigger Mode: AUTO
- b. Trigger Slope: +
- c. Trigger Coupling: DC
- d. Trigger Source: EXT
- e. Pre-trigger: ZERO

9.2.3. Channel A Controls

- a. On/Off: ON
- b. Save: OFF
- c. Volts Full Scale: 150 mV
- d. Input Coupling: DC
- e. DC Offset: Screen Center

9.2.4. Channel B Controls

- a. On/Off: OFF
 - b. Save: OFF
 - c. Volts Full Scale: 150 mV
 - d. Input Coupling: DC
 - e. DC Offset: Screen Center
-



ADC Board
Figure 9-1

9.3.0. CHANNEL A ADJUST

- 9.3.1. Connect the function generator's sync output to the EXT TRIG BNC and adjust the trigger LEVEL control for a stable trigger.
- 9.3.2. Input a 10 kHz square wave to the channel A input BNC via an RC network (Figure #2, page 10-2).
- 9.3.3. Adjust the generator output amplitude until the displayed square wave is approximately 1/2 of full scale.
- 9.3.4. Press the Hold Last button.
- 9.3.5. Press the channel A SAVE button.
- 9.3.6. Volts Full Scale: 1.5 V
- 9.3.7. Press the LIVE button.
- 9.3.8. Increase the generator output amplitude until the amplitudes of both waveforms on the screen are similar.

9.3.9.

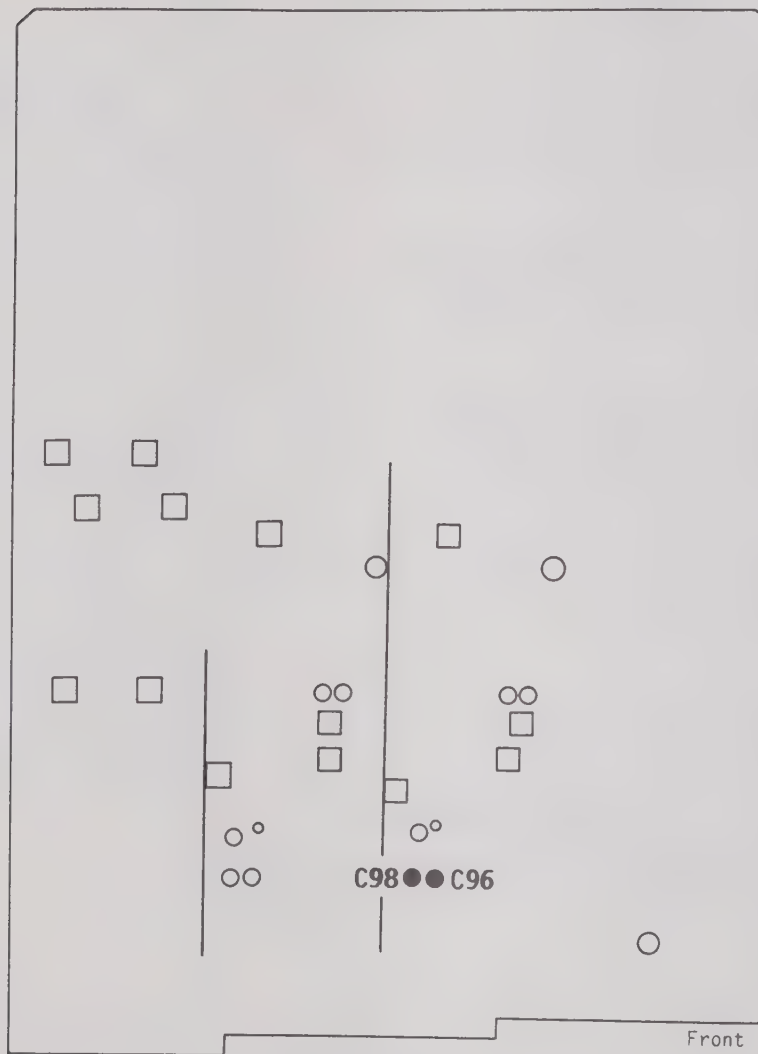
SPECIFICATION
If the slopes of the two waveforms differ, adjust capacitor C160 (Figure 9-1) until the slopes of both waveforms are identical.

9.3.10. Volts Full Scale: 15 V

- 9.3.11. Increase the generator output amplitude until the amplitudes of both waveforms on the screen are similar.

9.3.12.

SPECIFICATION
If the slopes of the two waveforms differ, adjust C158 (Figure 9-1) until the slopes of both waveforms are identical.



ADC Board
Figure 9-2

9.4.0. CHANNEL B ADJUST

9.4.1. Channel B on, channel A off.

9.4.2. Turn the channel A SAVE mode off.

9.4.3. Move the input signal from channel A to channel B.

9.4.4. Press the Live button.

9.4.5. Adjust the generator output amplitude until the displayed square wave is approximately 1/2 of full scale.

9.4.6. Press the Hold Last button.

9.4.7. Press the channel B SAVE button.

9.4.8. Volts Full Scale: 1.5 V

9.4.9. Increase the generator output amplitude until the amplitudes of both waveforms on the screen are similar.

9.4.10.

SPECIFICATION
If the slopes of the two waveforms differ, adjust capacitor C98 (Figure 9-2) until the slopes of both waveforms are similar.

9.4.11. Volts Full Scale: 15 V

9.4.12. Increase the generator output amplitude until the amplitudes of both waveforms on the screen are similar.

9.4.13.

SPECIFICATION
If the slopes of the two waveforms differ, adjust capacitor C96 (Figure 9-2) until the slopes of both waveforms on the screen are identical.

10.0.0. DC ADJUST

► **IMPORTANT:** The scope must be allowed to warm up fully with all covers in place before making this adjustment.

10.1.0. SET-UP

10.1.1. General Controls

- | | |
|--------------------------|--------|
| a. Power: | ON |
| b. Horizontal Expansion: | OFF |
| c. Vertical Expansion: | OFF |
| d. Autocenter: | ON |
| e. Display: | YT |
| f. Storage: | LIVE |
| g. Time Per Point: | 100 nS |

10.1.2. Trigger Controls

- | | |
|----------------------|------|
| a. Trigger Mode: | AUTO |
| b. Trigger Slope: | + |
| c. Trigger Coupling: | DC |
| d. Pre-trigger: | ZERO |
| e. Trigger Source: | EXT |

10.1.3. Channel A Controls

- | | |
|----------------------|---------|
| a. On/Off: | ON |
| b. Save: | OFF |
| c. Volts Full Scale: | 3V |
| d. Input Coupling: | GND |
| e. DC Offset: | OFF (*) |

10.1.4. Channel B Controls

- | | |
|----------------------|---------|
| a. On/Off: | OFF |
| b. Save: | OFF |
| c. Volts Full Scale: | 3V |
| d. Input Coupling: | GND |
| e. DC Offset: | OFF (*) |

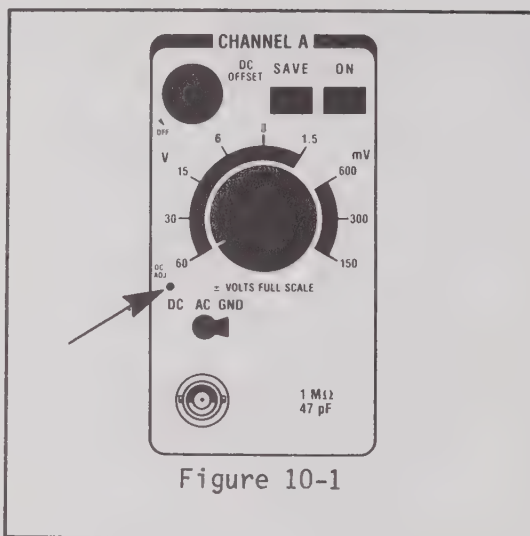


Figure 10-1

(*): Push in and turn fully counterclockwise.

10.2.0. CHANNEL A ADJUST

10.2.1. Adjust the channel A DC ADJ (Figure 10-1) until the channel A dc level is at screen center and the voltage numerics read 0.0V.

10.2.2. Push in the channel A DC OFFSET knob and slowly rotate it clockwise.

10.2.3.

SPECIFICATION

Confirm that the trace snaps to the bottom of the screen and the voltage numerics read -3.2768 V.

10.2.4. Continue rotating the channel A DC OFFSET knob in the clockwise direction.

10.2.5.

SPECIFICATION

Confirm that the trace snaps to the top of the screen and the voltage numerics read 3.2512 V.

10.3.0. CHANNEL B ADJUST

10.3.1. Channel B on, channel A off.

10.3.2. Adjust the channel B DC ADJ until the channel B dc level is at screen center and the voltage numerics read 0.0V.

10.3.3. Push in the channel B DC OFFSET knob and slowly rotate it clockwise.

10.3.4.

SPECIFICATION

Confirm that the trace snaps to the bottom of the screen and the voltage numerics read -3.2768 V.

10.3.5. Continue rotating the channel B DC OFFSET knob in the clockwise direction.

10.3.6.

SPECIFICATION

Confirm that the trace snaps to the top of the screen and the voltage numerics read 3.2512 V.

MNEMONICS

The signal connector list begins on page 11-3.

The mnemonics mapping list begins on page 11-23.

NOTE: The "-" sign at the end of a mnemonic identifies a "negated" command.

For example, RESET- = RESET.

320 CONNECTOR IDENTIFIER

CONNECTOR	PATH	PINS
J00	Ground Lug	1
J01	Input Power Module	8
J02	Input Power Switch	4
J03	Power Supply Inputs	6
J04	Pen Lift BNC	1
J05	X Pen BNC	1
J06	Y Pen BNC	1
J07	RS-232	25
J08	IEEE-488	24
J09	High Voltage - Mother Board	6
J10	CRT	11
J11	PDA (CRT Post Deflection Acceleration)	1
J12	Processor - Mother Board (Power)	64
J13	Power Supply - Mother Board	9
J14	Fan - Mother Board	2
J15	Processor - Mother Board (Signal)	200
J16	Mother - Rear Panel Board	60
J17	Mother - Remote Board	26
J19	Mother - ADC Board	160
J20	Mother - Bubble Memory Board	50
J21	Processor - Cursor Board	48
J22	ADC - Cursor Board	32
J23	ADC - Trigger Board	32
J25	Processor Test Address	20
J26	Processor Test Data	20
J27	Processor Test Status	20
J29	Offset to Trigger Board	14
J31	Time Per Point Switch to Trigger Board	6
J32	Pen Pot to Rear Board	10
J36	Display Amplifier to Mother Board	34

CONNECTOR/SIGNAL	DESCRIPTION
J00-01 GND	Ground
J01-01 THIRDPRONGGROUND	Third Prong Ground
J01-02 NEUTRAL	Neutral
J01-03 LINE	Line
J01-04 220SELECT*	220 Volt Select
J01-05 240SELECT	240 Volt Select
J01-06 120SELECT	120 Volt Select
J01-07 100SELECT*	100 Volt Select
J01-08 SW-FIL-LINE	Switch-Filter-Line
J02-01 SW-NEUTRAL	Switch-Neutral
J02-02 NEUTRAL	Neutral
J02-03 SW-LINE	Switch-Line
J02-04 LINE	Line
J03-01 SW-NEUTRAL	Switch-Neutral
J03-02 THIRDPRONGGROUND	Third Prong Ground
J03-03 120SELECT	120 Volt Select
J03-04 240SELECT	240 Volt Select
J03-05 SW-LINE	Switch-Line
J03-06 SW-FIL-LINE	Switch-Filter-Line
J04-01 PENLIFT	Pen Lift
J05-01 XPEN	X Pen
J06-01 YPEN	Y Pen
J07-01 OPEN	Open
J07-02 TDATA	RS232 Transmitted Data
J07-03 RDATA	RS232 Received Data
J07-04 RTS	RS232 Request To Send
J07-05 CTS	RS232 Clear To Send
J07-06 DSR	RS232 Data Set Ready
J07-07 GND	Ground
J07-08 CD	RS232 Carrier Detected
J07-09 OPEN	Open
J07-10 OPEN	Open
J07-11 OPEN	Open
J07-12 OPEN	Open
J07-13 OPEN	Open
J07-14 OPEN	Open
J07-15 OPEN	Open
J07-16 OPEN	Open
J07-17 OPEN	Open
J07-18 OPEN	Open
J07-19 OPEN	Open
J07-20 DTR	RS232 Data Terminal Ready
J07-21 OPEN	Open
J07-22 OPEN	Open
J07-23 OPEN	Open
J07-24 OPEN	Open
J07-25 OPEN	Open

CONNECTOR/MNEMONIC	DESCRIPTION
J08-01 IDAT1	IEEE Data 1
J08-02 IDAT2	IEEE Data 2
J08-03 IDAT3	IEEE Data 3
J08-04 IDAT4	IEEE Data 4
J08-05 EOI	IEEE End Or Identify
J08-06 DAV	IEEE Data Valid
J08-07 NRFD	IEEE Not Ready For Data
J08-08 NDAC	IEEE Not Data Accepted
J08-09 IFC	IEEE Interface Clear
J08-10 SRQ	IEEE Service Request
J08-11 ATN	IEEE Attention
J08-12 GND	Ground
J08-13 IDAT5	Ground
J08-14 IDAT6	Ground
J08-15 IDAT7	Ground
J08-16 IDAT8	Ground
J08-17 REN	IEEE Remote Enable
J08-18 GND	Ground
J08-19 GND	Ground
J08-20 GND	Ground
J08-21 GND	Ground
J08-22 GND	Ground
J08-23 GND	Ground
J08-24 GND	Ground
J09-01 +110V	+110 Volts DC
J09-02 HVBEAM-	High Voltage Beam
J09-03 GND	Ground
J09-04 GND	Ground
J09-05 +15	+15 Volts
J09-06 -15	-15 Volts
J10-01 H1 (BROWN)	CRT Pin H1 (Heater)
J10-02 K-INT (YELLOW w/RED)	CRT Pin K (Intensity)
J10-03 G1 (RED)	CRT Pin G1
J10-04 P1 (WHITE w/RED)	CRT Pin P1
J10-05 OPEN (WHITE w/GREEN)	Open
J10-06 P2 (YELLOW w/GREEN)	CRT Pin P1
J10-07 Y+ (GREEN)	CRT Pin Y+
J10-08 NONE	None
J10-09 Y- (BLACK)	CRT Pin Y-
J10-10 NONE	None
J10-11 X- (YELLOW w/BLUE)	CRT Pin X-
J10-12 G2 (BLUE)	CRT Pin G2
J10-13 X+ (WHITE w/BLUE)	CRT Pin X+
J10-14 H2 (BROWN)	CRT Pin H2 (Heater)
J11-01 PDA (BLACK)	CRT Pin PDA (Post Deflection Accelerator)
J12-01 GND	Ground
J12-02 XB	XDAC Data B

CONNECTOR/MNEMONIC	DESCRIPTION
J12-03 GND	Ground
J12-04 XA	XDAC Data A
J12-05 GND	Ground
J12-06 X9	XDAC Data 9
J12-07 GND	Ground
J12-08 X8	XDAC Data 8
J12-09 GND	Ground
J12-10 X7	XDAC Data 7
J12-11 GND	Ground
J12-12 X6	XDAC Data 6
J12-13 GND	Ground
J12-14 X5	XDAC Data 5
J12-15 GND	Ground
J12-16 X4	XDAC Data 4
J12-17 GND	Ground
J12-18 X3	XDAC Data 3
J12-19 GND	Ground
J12-20 X2	XDAC Data 2
J12-21 GND	Ground
J12-22 NC	No Connection
J12-23 GND	Ground
J12-24 NC	No Connection
J12-25 GND	Ground
J12-26 YB	YDAC Data B
J12-27 GND	Ground
J12-28 YA	YDAC Data A
J12-29 GND	Ground
J12-30 Y9	YDAC Data 9
J12-31 GND	Ground
J12-32 Y8	YDAC Data 8
J12-33 GND	Ground
J12-34 Y7	YDAC Data 7
J12-35 GND	Ground
J12-36 Y6	YDAC Data 6
J12-37 GND	Ground
J12-38 Y5	YDAC Data 5
J12-39 GND	Ground
J12-40 Y4	YDAC Data 4
J12-41 GND	Ground
J12-42 Y3	YDAC Data 3
J12-43 GND	Ground
J12-44 Y2	YDAC Data 2
J12-45 +5	+5 Volts
J12-46 NC	No Connection
J12-47 +5	+5 Volts
J12-48 NC	No Connection
J12-49 +5	+5 Volts

CONNECTOR/MNEMONIC	DESCRIPTION
J12-50	BEAM-
J12-51	+5
J12-52	YTG
J12-53	+5
J12-54	YTG-
J12-55	+15
J12-56	+15
J12-57	+15
J12-58	-15
J12-59	-15
J12-60	-15
J12-61	NC
J12-62	XPENADJ
J12-63	NC
J12-64	YPENADJ
J13-01	GND (GREY)
J13-02	PF- (VIOLET)
J13-03	+15(YELLOW)
J13-04	-5.2 (BLUE)
J13-05	GND (GREY)
J13-06	+5 (RED)
J13-07	-15 (ORANGE)
J13-08	+5 (RED)
J13-09	GND(GREY)
J14-01	GND
J14-02	+12
J15-01A	GND
J15-01B	BMTXRQ-*
J15-01C	BMTXAK-*
J15-01D	BMIRQ-*
J15-02A	GND
J15-02B	BMPF-
J15-02C	BMRESET-*
J15-02D	BMSCE-*
J15-03A	GND
J15-03B	N.C.
J15-03C	BMWR-
J15-03D	BMRD-
J15-04A	GND
J15-04B	BMD0
J15-04C	BMD1
J15-04D	BMD2
J15-05A	GND
J15-05B	BMD3
J15-05C	BMD4
J15-05D	BMD5
J15-06A	GND
	Beam
	+5 Volts
	YT Gain
	+5 Volts
	YT Gain
	+15 Volts
	+15 Volts
	+15 Volts
	-15 Volts
	-15 Volts
	-15 Volts
	No Connection
	X Pen Adjust
	No Connection
	Y Pen Adjust
	Ground
	Power Fail
	+15 Volts
	-5.2 Volts
	Ground
	+5 Volts
	-15 Volts
	+5 Volts
	Ground
	Ground
	+12 Volts
	Ground
	Bubble Memory Transfer Request
	Bubble Memory Transfer Acknowledge
	Bubble Memory Interrupt Request
	Ground
	Bubble Memory Power Fail
	Bubble Memory Reset
	Not Defined
	Ground
	No Connection
	Bubble Memory Write
	Bubble Memory Read
	Ground
	Bubble Memory Data Line 0
	Bubble Memory Data Line 1
	Bubble Memory Data Line 2
	Ground
	Bubble Memory Data Line 3
	Bubble Memory Data Line 4
	Bubble Memory Data Line 5
	Ground

CONNECTOR/MNEMONIC	DESCRIPTION
J15-06B BMD6	Bubble Memory Data Line 6
J15-06C BMD7	Bubble Memory Data Line 7
J15-06D A1(BMA0)	Bubble Memory Address Line 0
J15-07A GND	Ground
J15-07B A2(BMA1)	Bubble Memory Address Line 1
J15-07C A3(BMA2)	Bubble Memory Address Line 2
J15-07D BMCS-	Bubble Memory Chip Select
J15-08A GND	Ground
J15-08B +12	+12 Volts
J15-08C +12	+12 Volts
J15-08D +12	+12 Volts
J15-09A GND	Ground
J15-09B -12	-12 Volts
J15-09C -12	-12 Volts
J15-09D -12	-12 Volts
J15-10A GND	Ground
J15-10B A0MB	CPU Address Line 0 Mother Board (Buffered)
J15-10C GND*	Ground
J15-10D A1MB	CPU Address Line 1 Mother Board (Buffered)
J15-11A GND	Ground
J15-11B A2MB	CPU Address Line 2 Mother Board (Buffered)
J15-11C GND*	Ground
J15-11D A3MB	CPU Address Line 3 Mother Board (Buffered)
J15-12A GND	Ground
J15-12B A4MB	CPU Address Line 4 Mother Board (Buffered)
J15-12C GND*	Ground
J15-12D A5MB	CPU Address Line 5 Mother Board (Buffered)
J15-13A GND	Ground
J15-13B A6MB	CPU Address Line 6 Mother Board (Buffered)
J15-13C GND*	Ground
J15-13D A7MB	CPU Address Line 7 Mother Board (Buffered)
J15-14A GND	Ground
J15-14B A8MB	CPU Address Line 8 Mother Board (Buffered)
J15-14C A16MB	CPU Address Line 16 Mother Board (Buffered)
J15-14D A9MB	CPU Address Line 9 Mother Board (Buffered)
J15-15A GND	Ground
J15-15B A10MB	CPU Address Line 10 Mother Board (Buffered)
J15-15C A17MB	CPU Address Line 17 Mother Board (Buffered)
J15-15D A11MB	CPU Address Line 11 Mother Board (Buffered)
J15-16A GND	Ground
J15-16B A12MB	CPU Address Line 12 Mother Board (Buffered)
J15-16C A18MB	CPU Address Line 18 Mother Board (Buffered)
J15-16D A13MB	CPU Address Line 13 Mother Board (Buffered)
J15-17A GND	Ground
J15-17B A14MB	CPU Address Line 14 Mother Board (Buffered)
J15-17C A19MB	CPU Address Line 19 Mother Board (Buffered)
J15-17D A15MB	CPU Address Line 15 Mother Board (Buffered)

CONNECTOR/MNEMONIC	DESCRIPTION
J15-18A	DOMB
J15-18B	GND
J15-18C	ADC6
J15-18D	D1MB
J15-19A	GND
J15-19B	CAL/PLOT-
J15-19C	IEEE-EOI
J15-19D	GND*
J15-20A	D2MB
J15-20B	GND
J15-20C	IEEE-DAV
J15-20D	D3MB
J15-21A	GND
J15-21B	IEEE-NRFD
J15-21C	IEEE-NDAC
J15-21D	GND*
J15-22A	D4MB
J15-22B	GND
J15-22C	IEEE-IFC
J15-22D	D5MB
J15-23A	GND
J15-23B	IEEE-SRQ
J15-23C	IEEE-ATN
J15-23D	GND*
J15-24A	D6MB
J15-24B	GND
J15-24C	IEEE-REN
J15-24D	D7MB
J15-25A	GND
J15-25B	IDAT1
J15-25C	IDAT2
J15-25D	GND*
J15-26A	D8MB
J15-26B	GND
J15-26C	IDAT3
J15-26D	D9MB
J15-27A	GND
J15-27B	IDAT4
J15-27C	IDAT5
J15-27D	GND*
J15-28A	D10MB
J15-28B	GND
J15-28C	IDAT6
J15-28D	D11MB
J15-29A	GND
J15-29B	IDAT7
J15-29C	IDAT8
	CPU Data Line 0 Mother Board (Buffered)
	Ground
	Not Defined
	CPU Data Line 1 Mother Board (Buffered)
	Ground
	Calibrate/Plot
	IEEE End Or Identify
	Ground
	CPU Data Line 2 Mother Board (Buffered)
	Ground
	IEEE Data Valid
	CPU Data Line 3 Mother Board (Buffered)
	Ground
	IEEE Not Read For Data
	IEEE Not Data Accepted
	Ground
	CPU Data Line 4 Mother Board (Buffered)
	Ground
	IEEE Interface Clear
	CPU Data Line 5 Mother Board (Buffered)
	Ground
	IEEE Service Request
	IEEE Attention
	Ground
	CPU Data Line 6 Mother Board (Buffered)
	Ground
	IEEE Remote Enable
	CPU Data Line 7 Mother Board (Buffered)
	Ground
	IEEE Data 1
	IEEE Data 2
	Ground
	CPU Data Line 8 Mother Board (Buffered)
	Ground
	IEEE Data 3
	CPU Data Line 9 Mother Board (Buffered)
	Ground
	IEEE Data 4
	IEEE Data 5
	Ground
	CPU Data Line 10 Mother Board (Buffered)
	Ground
	IEEE Data 6
	CPU Data Line 11 Mother Board (Buffered)
	Ground
	IEEE Data 7
	IEEE Data 8

CONNECTOR/MNEMONIC	DESCRIPTION
J15-29D GND*	Ground
J15-30A D12MB	CPU Data Line 12 Mother Board (Buffered)
J15-30B GND	Ground
J15-30C IEEEEN-	IEEE Enable
J15-30D D13MB	CPU Data Line 13 Mother Board (Buffered)
J15-31A GND	Ground
J15-31B RS232EN-	RS232 Enable
J15-31C REFTIMER	Reference Timer
J15-31D GND*	Ground
J15-32A D14MB	CPU Data Line 14 Mother Board (Buffered)
J15-32B GND	Ground
J15-32C PENTIMER	Pen Timer
J15-32D D15MB	CPU Data Line 15 Mother Board (Buffered)
J15-33A GND	Ground
J15-33B PENLIFT	Pen Lift
J15-33C XPEN	X Pen
J15-33D GND*	Ground
J15-34A DT/RMB	CPU Data Transmit/Receive Mother Board
J15-34B GND	Ground
J15-34C YPEN	Y Pen
J15-34D IOSELECT-	Input/Output Select
J15-35A GND	Ground
J15-35B DTR	RS232 Data Terminal Ready
J15-35C DSR	RS232 Data Set Ready
J15-35D GND*	Ground
J15-36A PIINT1-	Plug-in Interrupt 1
J15-36B GND	Ground
J15-36C CD	RS232 Carrier Detected
J15-36D PIINTO-	Plug-in Interrupt 0
J15-37A WRMB-	Write Mother Board
J15-37B GND	Ground
J15-37C CTS	RS232 Clear To Send
J15-37D GND*	Ground
J15-38A RDMB-	Read Mother Board
J15-38B GND	Ground
J15-38C RTS	RS232 Request To Send
J15-38D GND*	Ground
J15-39A PI3EN-	Plug-in 3 Enable
J15-39B GND	Ground
J15-39C TDATA	RS232 Transmitted Data
J15-39D XPEAA	External Pulse External Address Advance
J15-40A PI2EN-	Plug-in 2 Enable
J15-40B GND	Ground
J15-40C RDATA	RS232 Received Data
J15-40D PI1EN-	Plug-in 1 Enable
J15-41A GND	Ground
J15-41B RETO (DIP SWITCH,REAR)	Return Line 0

CONNECTOR/MNEMONIC	DESCRIPTION
J15-41C	TRIG
J15-41D	OPEN2
J15-42A	MSIN
J15-42B	GND
J15-42C	RET1
J15-42D	MCS3MB-
J15-43A	GND
J15-43B	RET2
J15-43C	RET3
J15-43D	MSOUT
J15-44A	DRQ1-
J15-44B	GND
J15-44C	RET4
J15-44D	CHAEN-
J15-45A	GND
J15-45B	RET5
J15-45C	RET6
J15-45D	TIMEEN-
J15-46A	CHBEN-
J15-46B	GND
J15-46C	RET7
J15-46D	LIVE-
J15-47A	GND
J15-47B	+5
J15-47C	+5
J15-47D	STORE-
J15-48A	GND
J15-48B	I/OEN-
J15-48C	CUREN-
J15-48D	TIMEEN-
J15-49A	GND
J15-49B	ECLKEN-
J15-49C	ECUROUT-
J15-49D	ECLKIN-
J15-50A	GND
J15-50B	EXRSTIN-
J15-50C	ESWPGATE
J15-50D	ERAMPOUT
J16-01	+5
J16-02	+5
J16-03	RET7
J16-04	TIMEEN-
J16-05	RET6
J16-06	RET5
J16-07	RET4
J16-08	GND
J16-09	RET3
	Trigger
	Open 2
	Master Slave In
	Ground
	Return Line 1
	Mid Chip Select 3 Mother Board
	Ground
	Return Line 2
	Return Line 3
	Master Slave Out
	DMA Request
	Ground
	Return Line 4
	Channel A Enable
	Ground
	Return Line 5
	Return Line 6
	Time Per Point Enable
	Channel B Enable
	Ground
	Return Line 7
	Live
	Ground
	+5 Volts
	+5 Volts
	Store
	Ground
	Input/Output Enable
	Cursor Enable
	Time Per Point Enable
	Ground
	External Clock Enable
	External Cursor Out
	External Clock In
	Ground
	External Reset In
	External Sweep Gate
	External Ramp Out
	+5 Volts
	+5 Volts
	Return Line 7
	Time Per Point Enable
	Return Line 6
	Return Line 5
	Return Line 4
	Ground
	Return Line 3

CONNECTOR/MNEMONIC	DESCRIPTION
J16-10 RET2	Return Line 2
J16-11 RET1	Return Line 1
J16-12 GND	Ground
J16-13 LIVE-	Live
J16-14 RET0	Return Line 0
J16-15 RDATA	RS232 Received Data
J16-16 GND	Ground
J16-17 TDATA	RS232 Transmitted Data
J16-18 GND	Ground
J16-19 RTS	RS232 Request To Send
J16-20 GND	Ground
J16-21 CTS	RS232 Clear To Send
J16-22 GND	Ground
J16-23 CD	RS232 Carrier Detected
J16-24 GND	Ground
J16-25 DSR	RS232 Data Set Ready
J16-26 DTR	RS232 Data Terminal Read
J16-27 YPEN	Y Pen
J16-28 GND	Ground
J16-29 XPEN	X Pen
J16-30 PENLIFT	Pen Lift
J16-31 PENTIMER	Pen Timer
J16-32 GND	Ground
J16-33 REFTIMER	Reference Timer
J16-34 STORE-	Store
J16-35 CAL/PLOT-	Calibrate/Plot
J16-36 GND	Ground
J16-37 IDAT8	IEEE Data 8
J16-38 IDAT7	IEEE Data 7
J16-39 IDAT6	IEEE Data 6
J16-40 GND	Ground
J16-41 IDAT5	IEEE Data 5
J16-42 IDAT4	IEEE Data 4
J16-43 IDAT3	IEEE Data 3
J16-44 GND	Ground
J16-45 IDAT2	IEEE Data 2
J16-46 IDAT1	IEEE Data 1
J16-47 IEEE-REN	IEEE Remote Enable
J16-48 GND	Ground
J16-49 IEEE-ATN	IEEE Attention
J16-50 IEEE-SRQ	IEEE Service Request
J16-51 IEEE-IFC	IEEE Interface Clear
J16-52 GND	Ground
J16-53 IEEE-NDAC	IEEE Not Data Accepted
J16-54 IEEE-NRFD	IEEE Not Ready For Data
J16-55 IEEE-DAV	IEEE Data Valid
J16-56 GND	Ground

CONNECTOR/MNEMONIC		DESCRIPTION
J16-57	IEEE-EOI	IEEE End Or Identify
J16-58	I/OEN-	Input/Output Enable
J16-59	CUREN-	Cursor Enable
J16-60	GND	Ground
J17-01	XPEAA	External Pulse External Address Advance
J17-02	RET1	Return Line 1
J17-03	RET2	Return Line 2
J17-04	RET3	Return Line 3
J17-05	RET4	Return Line 4
J17-06	RET5	Return Line 5
J17-07	RET6	Return Line 6
J17-08	RET7	Return Line 7
J17-09	+5	+5 Volts
J17-10	+5	+5 Volts
J17-11	MSIN	Master/Slave In
J17-12	MSOUT	Master/Slave Out
J17-13	GND	Ground
J17-14	GND	Ground
J17-15	LIVE-	Live
J17-16	GND	Ground
J17-17	STORE-	Store
J17-18	I/OEN-	Input/Output Enable
J17-19	CUREN-	Cursor Enable
J17-20	TIMEEN-	Time Per Point Enable
J17-21	ECLKEN-	External Clock Enable
J17-22	ECUROUT-	External Cursor Out
J17-23	ECLKIN-	External Clock In
J17-24	EXRSTIN-	External Reset In
J17-25	ESWPGATE	External Sweep Gate
J17-26	ERAMPOUT	External Ramp Out
J19-01A	+15	+15 Volts
J19-01B	GND	Ground
J19-01C	+15	+15 Volts
J19-01D	+15	+15 Volts
J19-02A	+15	+15 Volts
J19-02B	GND	Ground
J19-02C	+15	+15 Volts
J19-02D	+15	+15 Volts
J19-03A	-15	-15 Volts
J19-03B	GND	Ground
J19-03C	-15	-15 Volts
J19-03D	-15	-15 Volts
J19-04A	-15	-15 Volts
J19-04B	GND	Ground
J19-04C	-15	-15 Volts
J19-04D	-15	-15 Volts
J19-05A	+5	+5 Volts

CONNECTOR/MNEMONIC	DESCRIPTION
J19-05B GND	Ground
J19-05C +5	+5 Volts
J19-05D +5	+5 Volts
J19-06A +5	+5 Volts
J19-06B GND	Ground
J19-06C +5	+5 Volts
J19-06D +5	+5 Volts
J19-07A +5	+5 Volts
J19-07B GND	Ground
J19-07C +5	+5 Volts
J19-07D +5	+5 Volts
J19-08A +5	+5 Volts
J19-08B GND	Ground
J19-08C +5	+5 Volts
J19-08D +5	+5 Volts
J19-09A -5	-5 Volts
J19-09B GND	Ground
J19-09C -5	-5 Volts
J19-09D -5	-5 Volts
J19-10A -5	-5 Volts
J19-10B GND	Ground
J19-10C -5	-5 Volts
J19-10D -5	-5 Volts
J19-11A AOMB	CPU Address Line 0 Mother Board (Buffered)
J19-11B GND	Ground
J19-11C GND*	Ground
J19-11D A1MB	CPU Address Line 1 Mother Board (Buffered)
J19-12A A2MB	CPU Address Line 2 Mother Board (Buffered)
J19-12B GND	Ground
J19-12C GND*	Ground
J19-12D A3MB	CPU Address Line 3 Mother Board (Buffered)
J19-13A A4MB	CPU Address Line 4 Mother Board (Buffered)
J19-13B GND	Ground
J19-13C GND*	Ground
J19-13D A5MB	CPU Address Line 5 Mother Board (Buffered)
J19-14A A6MB	CPU Address Line 6 Mother Board (Buffered)
J19-14B GND	Ground
J19-14C GND*	Ground
J19-14D A7MB	CPU Address Line 7 Mother Board (Buffered)
J19-15A A8MB	CPU Address Line 8 Mother Board (Buffered)
J19-15B GND	Ground
J19-15C A16MB	CPU Address Line 16 Mother Board (Buffered)
J19-15D A9MB	CPU Address Line 9 Mother Board (Buffered)
J19-16A A10MB	CPU Address Line 10 Mother Board (Buffered)
J19-16B GND	Ground
J19-16C A17MB	CPU Address Line 17 Mother Board (Buffered)
J19-16D A11MB	CPU Address Line 11 Mother Board (Buffered)

CONNECTOR/MNEMONIC	DESCRIPTION
J19-17A A12MB	CPU Address Line 12 Mother Board (Buffered)
J19-17B GND	Ground
J19-17C A18MB	CPU Address Line 18 Mother Board (Buffered)
J19-17D A13MB	CPU Address Line 13 Mother Board (Buffered)
J19-18A A14MB	CPU Address Line 14 Mother Board (Buffered)
J19-18B GND	Ground
J19-18C A19MB	CPU Address Line 19 Mother Board (Buffered)
J19-18D A15MB	CPU Address Line 15 Mother Board (Buffered)
J19-19A D0MB	CPU Data Line 0 Mother Board (Buffered)
J19-19B GND	Ground
J19-19C D1MB	CPU Data Line 1 Mother Board (Buffered)
J19-19D GND*	Ground
J19-20A D2MB	CPU Data Line 2 Mother Board (Buffered)
J19-20B GND	Ground
J19-20C D3MB	CPU Data Line 3 Mother Board (Buffered)
J19-20D GND*	Ground
J19-21A D4MB	CPU Data Line 4 Mother Board (Buffered)
J19-21B GND	Ground
J19-21C D5MB	CPU Data Line 5 Mother Board (Buffered)
J19-21D GND*	Ground
J19-22A D6MB	CPU Data Line 6 Mother Board (Buffered)
J19-22B GND	Ground
J19-22C D7MB	CPU Data Line 7 Mother Board (Buffered)
J19-22D GND*	Ground
J19-23A D8MB	CPU Data Line 8 Mother Board (Buffered)
J19-23B GND	Ground
J19-23C D9MB	CPU Data Line 9 Mother Board (Buffered)
J19-23D GND*	Ground
J19-24A D10MB	CPU Data Line 10 Mother Board (Buffered)
J19-24B GND	Ground
J19-24C D11MB	CPU Data Line 11 Mother Board (Buffered)
J19-24D GND*	Ground
J19-25A D12MB	CPU Data Line 12 Mother Board (Buffered)
J19-25B GND	Ground
J19-25C AINPULSE	Channel A In Pulse
J19-25D BINPULSE	Channel B In Pulse
J19-26A D13MB	CPU Data Line 13 Mother Board (Buffered)
J19-26B GND	Ground
J19-26C GND*	Ground
J19-26D D14MB	CPU Data Line 14 Mother Board (Buffered)
J19-27A 1MHZ	1 Megahertz
J19-27B GND	Ground
J19-27C 1MHZ-	1 Megahertz
J19-27D GND*	Ground
J19-28A D15MB	CPU Data Line 15 Mother Board (Buffered)
J19-28B GND	Ground
J19-28C GND*	Ground

CONNECTOR/MNEMONIC	DESCRIPTION
J19-28D DT/RMB	CPU Data Transmit/Receive Mother Board
J19-29A 2MHZ	2 Megahertz
J19-29B GND	Ground
J19-29C 2MHZ-	2 Megahertz
J19-29D GND*	Ground
J19-30A IOSELECT-	Input/Output Select
J19-30B GND	Ground
J19-30C GND*	Ground
J19-30D PIINT1-	Plug-in Interrupt 1
J19-31A CHAMEM	Channel A Memory
J19-31B GND	Ground
J19-31C CHBMEM	Channel B Memory
J19-31D CPUMEM	CPU Memory
J19-32A PIINTO-	Plug-in Interrupt 0
J19-32B GND	Ground
J19-32C WRMB-	Write Mother Board
J19-32D GND*	Ground
J19-33A RDMB-	Read Mother Board
J19-33B GND	Ground
J19-33C GND*	Ground
J19-33D PI3EN-	Plug-in 3 Enable
J19-34A TRIGLED-	Trigger LED
J19-34B GND	Ground
J19-34C RET0	Return Line 0
J19-34D RET1	Return Line 1
J19-35A XPEAA	External Pulse External Address Advance
J19-35B GND	Ground
J19-35C PI2EN-	Plug-in 2 Enable
J19-35D PI1EN-	Plug-in 1 Enable
J19-36A TRIG	Trigger
J19-36B GND	Ground
J19-36C OPEN2	Open 2
J19-36D MSIN	Master/Slave In
J19-37A MCS3MB-	Mid Chip Select 3 Mother Board
J19-37B GND	Ground
J19-37C MSOUT	Master/Slave Out
J19-37D DRQ1-	
J19-38A RET2	Return Line 2
J19-38B GND	Ground
J19-38C RET3	Return Line 3
J19-38D RET4	Return Line 4
J19-39A CHAEN-	Channel A Enable
J19-39B GND	Ground
J19-39C TIMEEN-	Time Per Point Enable
J19-39D CHBEN-	Channel B Enable
J19-40A RET5	Return Line 5
J19-40B GND	Ground

CONNECTOR/MNEMONIC	DESCRIPTION
J19-40C	RET6
J19-40D	RET7
J20-01	BMSCE-*
J20-02	N.C.
J20-03	BMRESET-*
J20-04	GND
J20-05	BMWR-
J20-06	GND
J20-07	BMRD-
J20-08	GND
J20-09	BMD7
J20-10	GND
J20-11	BMD6
J20-12	GND
J20-13	BMD5
J20-14	GND
J20-15	BMD4
J20-16	GND
J20-17	BMD3
J20-18	GND
J20-19	BMD2
J20-20	GND
J20-21	BMD1
J20-22	GND
J20-23	BMD0
J20-24	GND
J20-25	BMCS-
J20-26	GND
J20-27	BMIRQ-*
J20-28	GND
J20-29	BMTXRQ-*
J20-30	GND
J20-31	BMTXAK-*
J20-32	GND
J20-33	BMA2
J20-34	GND
J20-35	BMA1
J20-36	GND
J20-37	BMA0
J20-38	GND
J20-39	N.C.
J20-40	GND
J20-41	BMPF-
J20-42	GND
J20-43	+5
J20-44	+5
J20-45	+5

CONNECTOR/MNEMONIC	DESCRIPTION
J20-46 -12	-12 Volts
J20-47 +12	+12 Volts
J20-48 -12	-12 Volts
J20-49 +12	+12 Volts
J20-50 N.C.	No Connection
J21-01A TIMEEN-	Time Per Point Enable
J21-01B EXFNEN-	Expansion Functions Enable
J21-01C RET7	Return Line 7
J21-02A CHBEN-	Channel B Enable
J21-02B I/OEN-	Input/Output Enable
J21-02C RET6	Return Line 6
J21-03A CUREN-	Cursor Enable
J21-03B CHAEN-	Channel A Enable
J21-03C LED1-	LED 1
J21-04A OPEN	Open
J21-04B OPEN	Open
J21-04C OPEN	Open
J21-05A OPEN	Open
J21-05B RET0	Return Line 0
J21-05C RET2	Return Line 2
J21-06A OPEN	Open
J21-06B RET5	Return Line 5
J21-06C RET4	Return Line 4
J21-07A RET3	Return Line 3
J21-07B LED4-	LED 4
J21-07C RET1	Return Line 1
J21-08A AUTOLED-	Auto LED
J21-08B NORMLED-	Normal LED
J21-08C LED3-	LED 3
J21-09A CHAONLED-	Channel A ON LED
J21-09B CHBONLED-	Channel B ON LED
J21-09C I/OLED-	Input/Output LED
J21-10A VEXONLED-	Vertical Expansion ON LED
J21-10B CHASAVELED-	Channel A Save LED
J21-10C CHBSAVELED-	Channel B Save LED
J21-11A +12	+12 Volts
J21-11B HEXONLED-	Horizontal Expansion ON LED
J21-11C A.C.ONLED-	Autocenter ON LED
J21-12A +12	+12 Volts
J21-12B Y/TLED-	Y/T LED
J21-12C X/YLED-	X/Y LED
J21-13A +12	+12 Volts
J21-13B LED2-	LED 2
J21-13C GND	Ground
J21-14A +5	+5 Volts
J21-14B GND	Ground
J21-14C GND	Ground

CONNECTOR/MNEMONIC	DESCRIPTION
J21-15A +5	+5 Volts
J21-15B GND	Ground
J21-15C GND	Ground
J21-16A +5	+5 Volts
J21-16B GND	Ground
J21-16C GND	Ground
J22-01A TIMEEN-	Time Per Point Enable
J22-01B RET7	Return Line 7
J22-02A CHAONLED-	Channel A ON LED
J22-02B RET0	Return Line 0
J22-03A CHBONLED-	Channel B ON LED
J22-03B RET3	Return Line 3
J22-04A CHASAVELED-	Channel A Save LED
J22-04B RET1	Return Line 1
J22-05A CHBSAVELED-	Channel B Save LED
J22-05B RET2	Return Line 2
J22-06A TRIGLED-	Trigger LED
J22-06B RET4	Return Line 4
J22-07A GND	Ground
J22-07B GND	Ground
J22-08A GND	Ground
J22-08B GND	Ground
J22-09A +5	+5 Volts
J22-09B +5	+5 Volts
J22-10A RET6	Return Line 6
J22-10B +5	+5 Volts
J22-11A CHAEN-	Channel A Enable
J22-11B XCHBEN-(CHBEN-)	Jumper Channel B Enable (Channel B Enable)
J22-12A XCHAEN-(CHAEN-)	Jumper Channel B Enable (Channel B Enable)
J22-12B CHBEN-	Channel B Enable
J22-13A RET5	Return Line 5
J22-13B OPEN	Open
J22-14A OPEN	Open
J22-14B CHBON/OFF	Channel B On/Off
J22-15A CHBSAVE	Channel B Save
J22-15B CHAON/OFF	Channel A On/Off
J22-16A TEST0	Test 0
J22-16B CHASAVE	Channel A Save
J23-01A ATRIGE	Channel A Trigger (ECL)
J23-01B GND	Ground
J23-02A GND	Ground
J23-02B INTB	Channel B Internal Trigger
J23-03A INTA	Channel A Internal Trigger
J23-03B TMO	Time 0
J23-04A SET-UP	Set-up
J23-04B TM1	Time 1
J23-05A TM2	Time 2

CONNECTOR/MNEMONIC	DESCRIPTION
J23-05B -5	-5 Volts
J23-06A TM3	Time 3
J23-06B -2	-2 Volts
J23-07A TM4	Time 4
J23-07B -15	-15 Volts
J23-08A ZERO	Zero
J23-08B +15	+15 Volts
J23-09A GND	Ground
J23-09B GND	Ground
J23-10A GND	Ground
J23-10B OPEN	Open
J23-11A OPEN	Open
J23-11B BINPUT	Channel B Input
J23-12A GND	Ground
J23-12B OPEN	Open
J23-13A BOFFSET	Channel B Offset
J23-13B GND	Ground
J23-14A GND	Ground
J23-14B AOFFSET	Channel A Offset
J23-15A OPEN	Open
J23-15B GND	Ground
J23-16A AINPUT	Channel A Input
J23-16B OPEN	Open
J25-01 A13	CPU Address 13 (Test Header)
J25-02 A15	CPU Address 15 (Test Header)
J25-03 A9	CPU Address 9 (Test Header)
J25-04 A14	CPU Address 14 (Test Header)
J25-05 A10	CPU Address 10 (Test Header)
J25-06 A8	CPU Address 8 (Test Header)
J25-07 A11	CPU Address 11 (Test Header)
J25-08 A12	CPU Address 12 (Test Header)
J25-09 A6	CPU Address 6 (Test Header)
J25-10 A7	CPU Address 7 (Test Header)
J25-11 A5	CPU Address 5 (Test Header)
J25-12 A4	CPU Address 4 (Test Header)
J25-13 A2	CPU Address 2 (Test Header)
J25-14 A3	CPU Address 3 (Test Header)
J25-15 A0	CPU Address 0 (Test Header)
J25-16 A1	CPU Address 1 (Test Header)
J25-17 A16	CPU Address 16 (Test Header)
J25-18 A18	CPU Address 18 (Test Header)
J25-19 A17	CPU Address 17 (Test Header)
J25-20 A19	CPU Address 19 (Test Header)
J26-01 GND	Ground
J26-02 D15	CPU Data Line 15 (Test Header)
J26-03 GND	Ground
J26-04 D14	CPU Data Line 14 (Test Header)

CONNECTOR/MNEMONIC	DESCRIPTION
J26-05 D13	CPU Data Line 13 (Test Header)
J26-06 D12	CPU Data Line 12 (Test Header)
J26-07 D11	CPU Data Line 11 (Test Header)
J26-08 D10	CPU Data Line 10 (Test Header)
J26-09 D9	CPU Data Line 9 (Test Header)
J26-10 D8	CPU Data Line 8 (Test Header)
J26-11 +5	+5 Volts
J26-12 D7	CPU Data Line 7 (Test Header)
J26-13 D6	CPU Data Line 6 (Test Header)
J26-14 D5	CPU Data Line 5 (Test Header)
J26-15 D4	CPU Data Line 4 (Test Header)
J26-16 D3	CPU Data Line 3 (Test Header)
J26-17 D3	CPU Data Line 3 (Test Header)
J26-18 D1	CPU Data Line 1 (Test Header)
J26-19 D2	CPU Data Line 2 (Test Header)
J26-20 D0	CPU Data Line 0 (Test Header)
J27-01 CPUCLK ¹	CPU Clock (Buffered)
J27-02 RD	Read
J27-03 +5	+5 Volts
J27-04 GND	Ground
J27-05 +5	+5 Volts
J27-06 GND	Ground
J27-07 +5	+5 Volts
J27-08 GND	Ground
J27-09 +5	+5 Volts
J27-10 GND	Ground
J27-11 WR	Write
J27-12 BHE-	Byte Access
J27-13 S1-	Status 1
J27-14 S2-	Status 2
J27-15 OPEN	Open
J27-16 OPEN	Open
J27-17 S0-	Status 0
J27-18 RESET-	Reset
J27-19 OPEN	Open
J27-20 GND	Ground
J29-01 BRT	Channel B DC Reference Top
J29-02 BRB	Channel B DC Reference Bottom
J29-03 BOS1	Channel B DC Offset 1
J29-04 BOS2	Channel B DC Offset 2
J29-05 +8V	+8 Volts
J29-06 +8V	+8 Volts
J29-07 GND	Ground
J29-08 GND	Ground
J29-09 -8V	-8 Volts
J29-10 -8V	-8 Volts
J29-11 AOS2	Channel A DC Offset 2

CONNECTOR/MNEMONIC	DESCRIPTION
J29-12 AOS1	Channel A DC Offset 1
J29-13 ARB	Channel A DC Reference Bottom
J29-14 ART	Channel A DC Reference Top
J31-01 TMO	Time 0
J31-02 TM2	Time 2
J31-03 TM4	Time 4
J31-04 GND	Ground
J31-05 TM3	Time 3
J31-06 TM1	Time 1
J32-01 CAL/PLOT	Calibrate/Plot
J32-02 GND	Ground
J32-03 PP1	Pen Pot 1
J32-04 GND	Ground
J32-05 PPO	Pen Pot 0
J32-06 GND	Ground
J32-07 PPO	Pen Pot 0
J32-08 GND	Ground
J32-09 GND	Ground
J32-10 GND	Ground
J36-01 GND	Ground
J36-02 -0.6	-0.6 Volts
J36-03 -12	-12 Volts
J36-04 GND	Ground
J36-05 +6	+6 Volts
J36-06 -5	-5 Volts
J36-07 GND	Ground
J36-08 IY	YDAC Output Current
J36-09 IX	XDAC Output Current
J36-10 IX-N	XDAC Output Current Complement
J36-11 GND	Ground
J36-12 YR1	Y Rotation Pot 1
J36-13 YR2	Y Rotation Pot 2
J36-14 YP1	Y Position Pot 1
J36-15 YP2	Y Position Pot 2
J36-16 XR1	X Rotation Pot 1
J36-17 XR2	X Rotation Pot 2
J36-18 XP1	X Position Pot 1
J36-19 XP2	X Position Pot 2
J36-20 GND	Ground
J36-21 OPAMP-IN	Op Amp In
J36-22 OPAMP-OUT	Op Amp Out
J36-23 GND	Ground
J36-24 GND	Ground
J36-25 GND	Ground
J36-12 +12	+12 Volts
J36-27 +110V	+110 Volts DC
J36-28 -Y	Y Deflection

CONNECTOR/MNEMONIC	DESCRIPTION
J36-29 +110V	+110 Volts DC
J36-30 +Y	Y Deflection
J36-31 +110V	+110 Volts DC
J36-32 -X	X Deflection
J36-33 +110V	+110 Volts DC
J36-34 +X	X Deflection

MNEMONIC ABBREVIATIONS

The signal mnemonics (plus their originations/destinations) are listed in numerical/alphabetical order on the following pages. The abbreviations used to identify the originations and destinations are explained below.

NOTE: The "-" sign at the end of a mnemonic identifies a "negated" command.

For example, RESET - = $\overline{\text{RESET}}$

ABBREVIATION	DEFINITION
BM	Bubble memory holder
CRT	Cathode ray tube
CURSOR	Cursor board
DA	Display Amplifier board
DCO	DC Offset board (part of Trigger board)
FUSE HLDR	Fuse holder/Voltage selector
GND LUG	Ground lug for chassis ground
HV	High Voltage board
IEEE	Rear Panel IEEE 488 Connector
MOTHER	Mother board
PEN	Rear Panel Pen output BNC connectors
PEN POT	Pen Pot board (part of Rear Panel board)
PROC	Processor board
PS	Power supply
PWR SW	Power switch
RC	Remote Control board
RP	Rear panel board
RS-232	Rear panel RS-232 connector
T/P	Time/Point board (part of Trigger board)
TRIGGER	Trigger board
*	Signal does not leave board.

MMEMONIC	DEFINITION	ORIGINATES	DESTINATION
+110V	Positive 110 volt supply	HV	MOTHER, DA
+12	Positive 12 volt supply	MOTHER	DA
+15	Positive 15 volt supply	PS	various
+4000V	CRT anode voltage	HV	CRT
+5.4V	Positive 5.4 volt supply	TRIGGER	*
+6	Positive 6 volt supply	MOTHER	DA
+6A, -6A	Channel A supply voltages	ADC	*
+6B, -6B	Channel B supply voltages	ADC	*
+8V, -8V	Trigger board supply voltages	TRIGGER	TRIGGER, DCO
+VCCLED	FP LED supply voltage	PROC	CURSOR
+X	Horizontal deflection signal	DA	CRT
+Y	Vertical deflection signal	DA	CRT
-0.6	Negative 0.6 volt bias	DA	MOTHER
-12	Negative 12 volt supply	MOTHER	DA
-1300V	CRT cathode supply voltage	HV	*
-1306V	Blanking circuit supply voltage	HV	*
-1325V	CRT grid cut-off voltage	HV	*
-15	Negative 15 volt supply	PS	various
-2V	ECL termination voltage	ADC	*
-2V REF A	Channel A ADC reference voltage	ADC	*
-2V REF B	Channel B ADC reference voltage	ADC	*
-2X	-2 volt supply for 200 MHz clock osc.	ADC	*
-5	Negative 5 volt supply	MOTHER	DA
-5.2V	-5.2 volt supply for ECL	PS	ADC, TRIG
-X	Horiz. deflection invert	DA	CRT
-Y	Vertical deflection invert	DA	CRT
0 ADDR MTCH-	Address Match 0 (not used)	ADC	*
1 ADDR MTCH-	Address Match 1 (not used)	ADC	*
1 MHz, 1 MHz-	1 MHz display clock	PROC	*
100NS, 100NS-	10 MHz Clock	ADC	*
100SELECT	100 Volt Line select (not used)		
110	Positive 110 volt supply	HV	MOTHER, DA
120SELECT	120 Volt Line select	FUSE HLDR	PWR SW
16 MHz	16 MHz clock	PROC	*
2 MHz, 2 MHz-	2 MHz display clock	PROC	*
200 MHz	200 MHz prescaler clock	ADC	*
220SELECT	220 Volt Line select (not used)		
240SELECT	240 Volt Line Select	FUSE HLDR	PWR SW
4 MHz	4 MHz display clock	PROC	*
488 INT	IEEE 488 Interrupt	PROC	*
488 REQ-	IEEE 488 DMA request (not used)	PROC	*
488CLK	4 MHz Clock for IEEE 488 interface	PROC	*
50 nS, 50 nS-	20 MHz clock	ADC	*
8 MHz	8 MHz display clock	PROC	*
8051 INT	8051 Interrupt to CPU	PROC	*
8051 RD-	CPU Read from 8051	PROC	*
A ANALOG IN	Channel A signal to ADC chip	ADC	*

MNEMONIC	DEFINITION	ORIGINATES	DESTINATION
A INPUT	Channel A signal input	TRIGGER	ADC
A OFFSET	Channel A Offset voltage	TRIGGER	ADC
A SAMPLE	Channel A Sample/Hold clock	ADC	*
A SAMPLE-	Channel A Sample/Hold clock	ADC	*
A TRIG	Main sweep trigger pulse	ADC	*
A TRIG E	Main sweep trigger, ECL	TRIGGER	*
A.C. ON LED-	Autocenter on LED	PROC	CURSOR
A/B-	Channel A/Channel B memory select	ADC	*
AO to A19	CPU Address Bus, demultiplexed	PROC	*
AOMB to A19MB	Buffered Address Bus, Mother Board	PROC	ADC, BM
ADO to AD15	CPU Address/Data Bus, multiplexed	PROC	*
ADO to AD7	Channel A ADC data	ADC	*
ADC CLK	10 MHz ADC Clock	ADC	*
ADC INT	ADC Interrupt	ADC	*
ADC6	Undefined		
AINPULSE	Not Used		
ALE'	Address Latch Enable	PROC	*
AORO to AOR5	Address Offset Register (Prescaler out)	ADC	*
AOS1	Channel A offset voltage 1	DCO	TRIGGER
AOS2	Channel A offset voltage 2 (not used)	DCO	N/C
ARB	Channel A position pot, bottom	TRIGGER	DCO
ART	Channel A position pot, top	TRIGGER	DCO
ASA	Advance scratch memory address	ADC	*
ATN	IEEE 488 Attention	IEEE	PROC
AUTO	Output of auto trigger timer	ADC	*
AUTO LED-	Auto trigger LED	PROC	CURSOR
AXA	Advance XA counter	ADC	*
B ANALOG IN	Channel B signal to ADC chip	ADC	*
B INPUT	Channel B signal input	TRIGGER	ADC
B OFFSET	Channel B Offset voltage	TRIGGER	ADC
B RESET	Buffered ADC reset	ADC	*
B SAMPLE	Channel B Sample/Hold clock	ADC	*
B SAMPLE-	Channel B Sample/Hold clock	ADC	*
BADR5,6	Buffered CPU Address lines	ADC	*
BDO to BD7	Channel B ADC data	ADC	*
BEAA	Buffered EAA pulses	ADC	*
BEAM KILL-	Master Beam Kill	PROC	*
BEAM-	CRT beam control	PROC	MOTHER
BEEP-	Enable beep oscillator	PROC	*
BHE'-	Byte High Enable	PROC	*
BHE-	Byte High Enable, latched	PROC	*
BINPULSE	Not Used		
BMAO to BMA4	Address lines to Bubble Memory	PROC	BM
BMCS-	Bubble Memory Chip Select	PROC	BM
BMDO to BMD7	Buffered Data Bus, Bubble Memory	PROC	BM
BMIRQ-	BM Interrupt Request (not used)	BM	PROC
BMPF-	Bubble Memory Power Fail	CPU	BM

MNEMONIC	DEFINITION	ORIGINATES	DESTINATION
BMRD-	Bubble Memory Read	PROC	BM
BMRESET-	Bubble Memory Reset	PROC	BM
BMSCE-	BM Special commands enable (not used)	MOTHER	BM
BMT REQ-	BM DMA transfer request (not used)	BM	PROC
BMTXAK-	BM Transfer Acknowledge (not used)	PROC	BM
BMTXRQ-	BM Transfer Request (not used)	BM	PROC
BMWR-	Bubble Memory Write	PROC	BM
BOS1	Channel B offset voltage 1	DCO	TRIGGER
BOS2	Channel B offset voltage 2 (not used)	DCO	N/C
BPI1EN-	Buffered Plug-in 1 Enable	ADC	*
BRB	Channel B position pot, bottom	TRIGGER	DCO
BRT	Channel B position pot, top	TRIGGER	DCO
BTRIG	Buffered trigger pulse	ADC	*
CAL/PLOT-	Pen calibrate/plot switch	RP	PROC
CAR DN-	Carry down from XA counter	ADC	*
CAR UP-	Carry up from XA counter	ADC	*
CAS-	Display memory Column Address Strobe	PROC	*
CD	RS-232 Carrier Detect	RS-232	PROC
CHA ON LED-	Channel A on LED	PROC	CURSOR
CHA ON/OFF	Channel A on/off switch	CURSOR	ADC
CHA SAVE	Channel A Save Reference switch	CURSOR	ADC
CHA SAVE LED-	Channel A SAVE on LED	PROC	CURSOR
CHAEN-	Enable Channel A group of FP switches	PROC	ADC
CHAMEM	Channel A Memory (not used)		
CHB ON LED-	Channel B on LED	PROC	CURSOR
CHB ON/OFF	Channel B on/off switch	CURSOR	ADC
CHB SAVE	Channel B Save Reference switch	CURSOR	ADC
CHB SAVE LED-	Channel B SAVE on LED	PROC	CURSOR
CHBEN-	Enable Channel B group of FP switches	PROC	CURSOR, ADC
CHBMEM	Channel B Memory (not used)		
CMUX-	Display memory MUX (row/column addr.)	PROC	*
COMMAND WR-	Write command to XA counter	ADC	*
CPU CLK	8 MHz clock from CPU	PROC	*
CPU EN	Display memory enable CPU access	PROC	*
CPU REQ	Display memory CPU Request	PROC	*
CPUMEM	CPU Memory (not used)		
CS488-	IEEE 488 Chip Select	PROC	*
CS8051-	8051 Chip Select	PROC	*
CSBM'-	CPU Bubble Memory Chip Select	PROC	*
CSBM-	Buffered Bubble Memory Chip Select	PROC	*
CSLED	LED Latch Chip Select	PROC	*
CTS	RS-232 Clear to Send	RS-232	PROC
CUREN-	Enable cursor group of FP switches	PROC	CURSOR
CURSOR WR-	Write cursor trigger address	ADC	*
DO to D15	CPU Data Bus, demultiplexed	PROC	*
DOMB to D15MB	Buffered Data Bus, Mother Board	PROC	ADC
DAO to DA7	Display memory address, multiplexed	PROC	*

MNEMONIC	DEFINITION	ORIGINATES	DESTINATION
DATA RD- (ADC)	Data read (enable scratch RAM)	ADC	*
DATA RD- (CPU)	Waveform memory Read	PROC	*
DATA SRDY	Waveform memory Ready, synchronized	PROC	*
DATA WR-	Waveform memory Write	PROC	*
DAV	IEEE 488 Data Valid	IEEE	PROC
DELAY	Delay trigger enable	ADC	*
DELAY RD-	Read delay timer	ADC	*
DELAY WR-	Write to delay timer	ADC	*
DEN-	CPU Data Enable	PROC	*
DIS CLK	16 MHz Display Clock	PROC	*
DIS SRDY	Display memory Ready, Synchronized	PROC	*
DIS SRDY'	Display memory Ready	PROC	*
DIS SRDY'-	Display memory Ready, invert	PROC	*
DM11 to DM15	Display memory address, MSB's	PROC	*
DRQO-, DRQ1-	DMA Request (not used)	N/C	PROC
DSR	RS-232 Data Set Ready	RS-232	PROC
DT/R-	CPU Data Transmit/Receive	PROC	*
DT/RMB-	Data Xmit/Rcv., Mother Board (not used)	PROC	N/C
DTR	RS-232 Data Terminal Ready	PROC	RS-232
DTRGEN	Dithered Trigger Enable	ADC	*
DTRIG	Trigger pulse to delay counter	ADC	*
DWELL RD-	Read dwell timer	ADC	*
DWELL WR-	Write to dwell timer	ADC	*
DWEN	Dwell counter enable	ADC	*
EAA	External Address Advance enable	ADC	*
ECLKEN-	External Clock Enable (not used)		
ECLKIN-	External Clock In (not used)		
ECUROUT-	External Cursor Out (not used)		
EO, EO-	Even/Odd Sweep	ADC	*
EOI	IEEE 488 End Or Identify	IEEE	PROC
ERAMPOUT	External Ramp Out (not used)		
ESWPGATE	External Sweep Gate (not used)		
EXFNEN-	Enable Function group of FP switches	PROC	CURSOR
EXRSTIN-	External reset In (not used)		
G1	CRT grid 1	HV	CRT
G2	CRT grid 2	MOTHER	CRT
GND	Chassis Ground	GND LUG	PS
GO	Display state machine control	PROC	*
H.V. BEAM-	CRT beam control	MOTHER	HV
H1, 2	CRT heater voltage	HV	CRT
HEX ON LED-	Horizontal Expansion LED	PROC	CURSOR
I/O EN-	Enable I/O group of FP switches	PROC	CURSOR
I/O LED-	FP I/O LED	PROC	CURSOR
IDAT1 - IDAT8	IEEE 488 data lines	IEEE	PROC
IEEE EN-	Enable IEEE DIP switch	PROC	MOTHER

MNEMONIC	DEFINITION	ORIGINATES	DESTINATION
IFC	IEEE 488 Interface Clear	IEEE	PROC
INT A	Channel A Internal trigger signal	ADC	TRIGGER
INT B	Channel B Internal trigger signal	ADC	TRIGGER
IOSELECT-	Data Bus Direction, In/Out (not used)	PROC	N/C
IOWRT	Buffered CPU Write	ADC	*
IX, IX-	Horiz. deflection current from DAC	MOTHER	DA
IY, IY-	Vertical deflection current from DAC	MOTHER	DA
JA0, 1	ADC state machine Jump select	ADC	*
K	CRT cathode	HV	CRT
LED1-	Hold Next LED	PROC	CURSOR
LED2-	Dot Join LED	PROC	CURSOR
LED3-	Hold Last LED	PROC	CURSOR
LED4-	Live LED	PROC	CURSOR
LINE	AC Line Voltage In	FUSE HLDR	PWR SW
LIVE-	Live	PROC	RC
MA0 to MA7	Channel A scratch memory bus	ADC	*
MB0 to MB7	Channel B scratch memory bus	ADC	*
MCS0-	Memory Chip Select 0 (Static RAM)	PROC	*
MCS1-	Memory Chip Select 1 (Waveform Memory)	PROC	*
MCS2-	Memory Chip Select 2 (Display Memory)	PROC	*
MCS2/MCS3	MCS2 OR MCS3 (Display memory addressed)	PROC	*
MCS3-	Memory Chip Select 3 (Display Memory)	PROC	*
MSIN	Master-Slave in	RC	ADC
MSOUT	Master-Slave out	ADC	RC
NDAC	IEEE 488 Not Data Accepted	IEEE	PROC
NEUTRAL	AC Line Voltage In, Neutral	FUSE HLDR	PWR SW
NORM LED-	Normal trigger LED	PROC	CURSOR
NRFD	IEEE 488 Not Ready For Data	IEEE	PROC
OBL	On-board Latch	PROC	*
OP AMP IN	X deflection op amp input	MOTHER	DA
OP AMP OUT	X deflection op amp output	MOTHER	DA
OUT3 to OUT6	XA counter outputs (not used)	ADC	*
P1	CRT focus voltage	HV	CRT
P2	CRT astigmatism voltage	MOTHER	CRT
PD6 to PD15	ADC Board (Plug-in) data bus	ADC	*
PDA	CRT Anode Voltage	HV	CRT
PDATA RD-	ADC Data read	ADC	*
PEN LIFT	Pen Lift for XY recorder	PROC	PEN
PEN-TIMER	Pen timer oscillator	RP	PROC
PF-	Power Fail	PS	PROC
PI INT 0-	Plug-in 0 Interrupt (ADC board)	ADC	PROC
PI INT 1-	Plug-in 1 Interrupt (not used)	N/C	PROC
PI1EN'-	CPU Plug-in 1 Enable	PROC	*
PI1EN-	Plug-in 1 Enable	PROC	N/C
PI2EN'-	CPU Plug-in 2 Enable	PROC	*
PI2EN-	Plug-in 2 Enable (not used)	PROC	N/C

MNEMONIC	DEFINITION	ORIGINATES	DESTINATION
PI3EN'-	CPU Plug-in 3 Enable	PROC	*
PI3EN-	Plug-in 3 Enable (not used)	PROC	N/C
POWER-UP	Power-up reset to prescaler	ADC	*
PPO, PP1	Pen pot leads	PEN POT	RP
PTRIG	XTRIG delayed by 100 ns	ADC	*
PTRIG-	XTRIG- delayed by 100 ns	ADC	*
PU	Pull up to +5V	ADC	*
R/W	Display memory Read/Write	PROC	*
R/W ENA	Display memory Read/Write Enable	PROC	*
RO to R4	Beam intensity control	PROC	*
RAS-	Display memory Row Address Strobe	PROC	*
RD'-	CPU Read	PROC	*
RD, RD-	Buffered CPU Read	PROC	*
RDO-	Display memory Read 0 (Y coordinate)	PROC	*
RD1-	Display memory Read 1 (X coordinate)	PROC	*
RDATA	RS-232 Receive data	RS-232	PROC
RDL-	Read & latch display memory, X coord.	PROC	*
RDMB-	Buffered CPU Read, Mother Board	PROC	ADC
RDU-	Read & latch display memory, Y coord.	PROC	*
REFTIMER	Reference Timer (not used)	RP	N/C
REN	Remote Enable	IEEE	PROC
RESET (ADC)	ADC reset	ADC	*
RESET (CPU)	Synchronized reset from CPU	PROC	*
RESET- (CPU)	Buffered Reset from CPU	PROC	*
RETO to RET7	Switch return lines	various	PROC
RS232 EN-	Enable RS-232 DIP switch	PROC	MOTHER
RTS	RS-232 Request to Send	PROC	RS-232
S0- to S2-	CPU status lines	PROC	*
SA0 to SA11	Scratch memory addresses	ADC	*
SET UP	Trigger setup switch	TRIGGER	ADC
SLOW	Slow sweep speed (point-by-point dump)	ADC	*
SRQ	IEEE 488 Service Request	IEEE	PROC
STAT RD-	Read ADC status register	ADC	*
STOP	Display state machine control	PROC	*
STORE-	Store (Hold Last)	PROC	RC
SW-FIL-LINE	Switched Line Voltage	FUSE HLDR	PS
SW-LINE	Switched Line Voltage	PWR SW	PS
SW-NEUTRAL	Switched Line Voltage, Neutral	PWR SW	PS
SWP1	Sweep 1 (Data collection time)	ADC	*
SWPDONE	Sweep done	ADC	*
T GATE/E	Trigger Gate, ECL	ADC	*
TDATA	RS-232 Transmit data	PROC	RS-232
TESTO	Connected to CHAEN- at ADC board	CURSOR	ADC
THIRDPRONGGND.	AC Line Third Prong Ground	FUSE HLDR	PS
TICK	8 MHz display clock	PROC	*

MNEMONIC	DEFINITION	ORIGINATES	DESTINATION
TIME EN-	Enable T/P group of FP switches	PROC	CURSOR, ADC
TMO to TM4	Time per Point switch	T/P	ADC
TRG/DWL	Trigger or Dwell	ADC	*
TRGEN	Trigger Enable	ADC	*
TRGEN-E	Trigger Enable, ECL	ADC	*
TRIG LED-	Trigger LED	ADC	CURSOR
UCS-	Upper address Chip Select (EPROM)	PROC	*
UP	Pull up to +5V	PROC	*
URET-	Select Upper Return lines from FP sw.	PROC	*
VBIAS	-0.6V from voltage divider	TRIGGER	*
VEX ON LED-	Vertical Expansion LED	PROC	CURSOR
VFAST	Very Fast	ADC	*
WE-	Scratch memory Write	ADC	*
WR'-	CPU Write	PROC	*
WR, WR-	Buffered CPU Write	PROC	*
WRO-	Display memory Write 0 (Y coordinate)	PROC	*
WR1-	Display memory Write 1 (X coordinate)	PROC	*
WRMB-	Buffered CPU Write, Mother Board	PROC	ADC
X TRIG	Main or delay trigger	ADC	*
X TRIG-	Main or delay trigger	ADC	*
X/Y LED-	X/Y display LED	PROC	CURSOR
X2 to XB	Horizontal position data, 10 bits	PROC	MOTHER
XALOAD	Load X-axis Address counter	ADC	*
XAU/D-	XA count up/down	ADC	*
XCHAEN-	Connected to CHAEN- at ADC board	ADC	CURSOR
XCHBEN-	Connected to CHBEN- at ADC board	ADC	CURSOR
XP1, XP2	Horizontal position pot	MOTHER	DA
XPEAA	External Pulse for EAA	RC	ADC
XPEN	X output to pen recorder	PROC	PEN
XPENADJ	X pen offset adjust	MOTHER	PROC
XR1, XR2	Horizontal rotation pot	MOTHER	DA
Y/T LED-	Y/T display LED	PROC	CURSOR
Y2 to YB	Vertical position data, 10 bits	PROC	MOTHER
YDWELL	Dwell timer output (time per point)	ADC	*
YP1, YP2	Vertical position pot	MOTHER	DA
YPEN	Y output to pen recorder	PROC	PEN
YPENADJ	Y pen offset adjust	MOTHER	PROC
YR1, YR2	Vertical rotation pot	MOTHER	DA
YTG, YTG-	Y/T Gain control	PROC	MOTHER
ZO to Z7	Beam control - blank segment if false	PROC	*
ZERO	Trigger zero switch	TRIGGER	ADC
ZTRIG	Main or delay trigger	ADC	*

RENEWAL PARTS INDEX

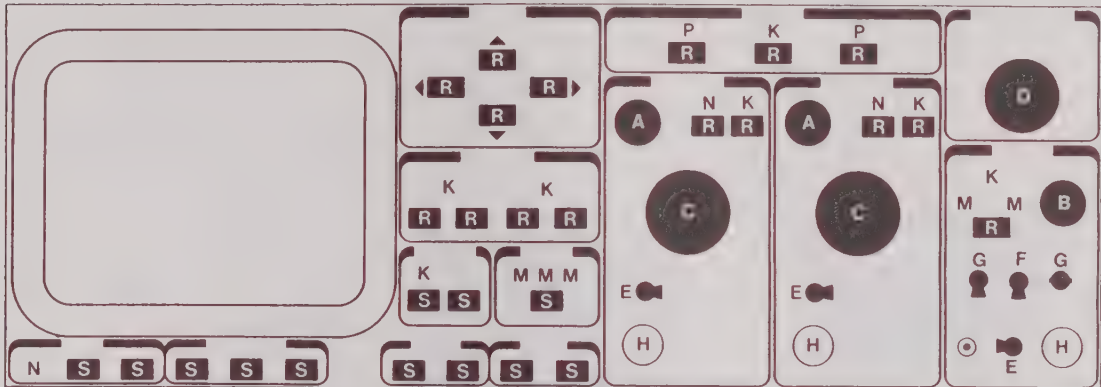
320 RENEWAL PARTS LIST INDEX			
DESCRIPTIONS		PAGE	
QUICK-FIND INDEX			
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PARTS LIST EXAMPLE

320 REAR PANEL & BOTTOM COVER ASSEMBLIES

RELATIVE LEVEL	COMPONENT ITEM NO.	DESCRIPTION (Truncated)	QTY (Each)
1	447-002200	320 BOTTOM COVER ASSEMBLY	1.000
*2	617-001400	3XX REAR PANEL ASSEMBLY	1.000
**3	417-002600	3XX PEN POT ASSEMBLY	1.000
***4	000-915900	PCB/300 PEN POT	1.000
***4	024-797300	CON 5M HDR/SOL S/RA	1.000
		Main Assembly	
		Subassembly	
		Design revision level.	
		Component on the Pen Pot circuit board.	
		Unassembled Pen Pot circuit board P/N.	
		Assembled circuit board P/N listed on the diagrams & etched on the circuit board.	

320 FRONT PANEL CONTROLS



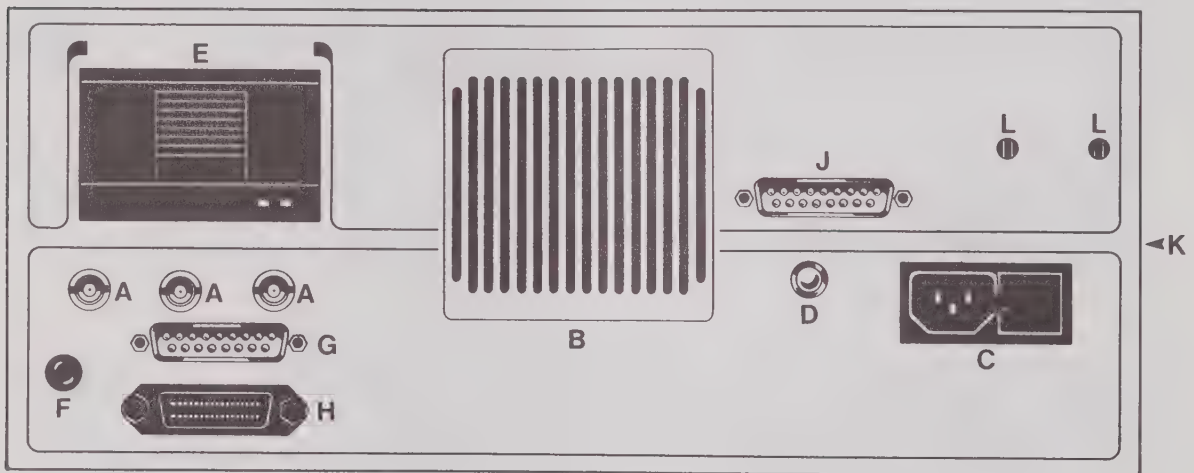
ITEM	DESCRIPTION	PART NUMBER	ITEM	DESCRIPTION	PART NUMBER
A	Potentiometer Knob	026-9000-01 045-9008-00	F	Switch (Tog) Knob	025-7512-00 035-7048-00
B	Potentiometer Knob	026-9003-02 045-9007-00	G	Switch (Tog) Knob	025-7513-00 035-7048-00
C	Switch (Rot) Knob	025-9002-01 045-9005-00	H	Input BNC	024-9003-00
D	Switch (Rot) Knob	025-9004-02 045-9006-00	K	LED (Green)	022-7246-00
E	Switch (Tog) Knob	025-7511-00 035-7048-00	M	LED (Yellow)	022-7247-00
			N	LED (Red)	022-7248-00
			P	LED (Red)	022-7249-00
			*	Pushbuttons	See Table 2

Table #1

ITEM	DESCRIPTION	PART NUMBER
-	Pushbutton Circuit Pads (one piece)	035-9000-04
R	Pushbutton Operators (one piece)	035-9001-00
S	Pushbutton Operators (one piece)	035-9002-00

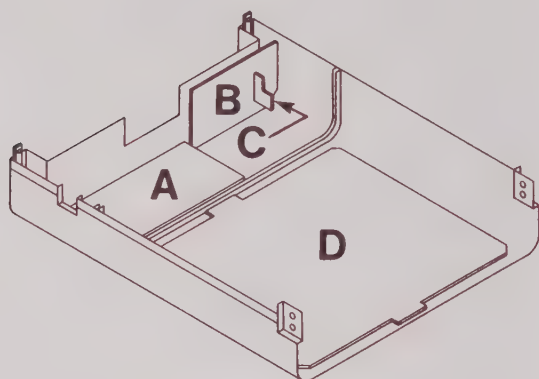
Table #2

320 REAR PANEL CONTROLS

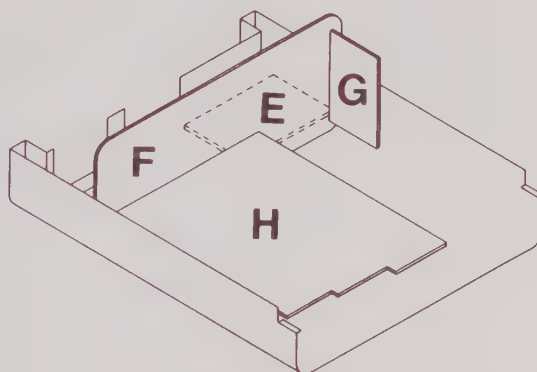


ITEM	DESCRIPTION	PART NUMBER	ITEM	DESCRIPTION	PART NUMBER
A	Input BNC	024-9003-00	G	Connector	024-7973-00
B	Fan	072-7024-00	H	Connector	024-8005-00
C	Fuse Holder	070-7088-00	J	Connector	024-7973-00
D	Post	060-7036-00	L	Pot	026-7176-00
E	Bubble Memory	222-0408-00	K	Power Switch	025-7509-00
F	Potentiometer Knob	026-9001-01 045-7052-00			

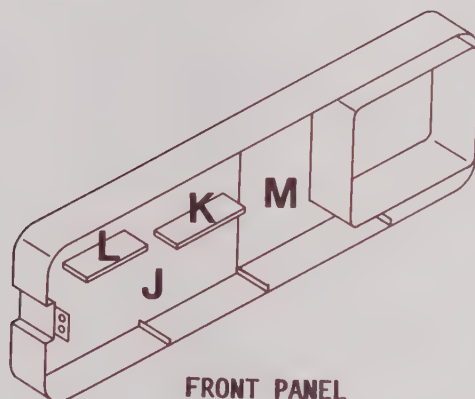
320 STANDARD BOARDS



BOTTOM COVER



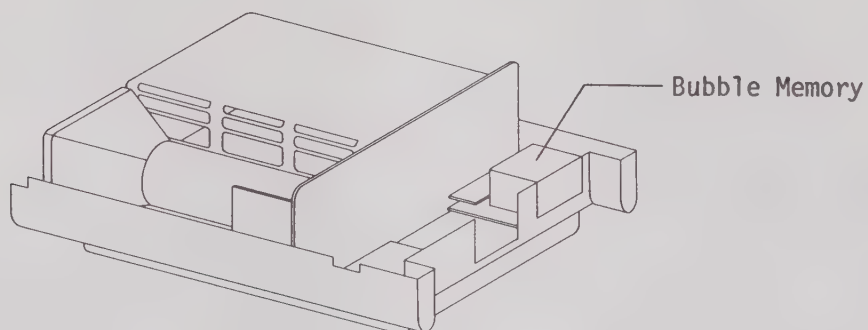
TOP COVER



FRONT PANEL

ITEM	DESCRIPTION	ASSEMBLED BOARD	COMPONENTS	DIAGRAMS
A	Power Supply Board	113-7075-00	12-9	-
B	Rear Panel Board	617-0014-00	12-9	14-31
C	Pen Pot Board	417-0026-00	12-9	14-31
D	Processor Board	617-0007-00	12-15	14-19
E	High Voltage Board	617-0008-00	12-10	14-29
F	Mother Board	617-0006-00	12-14	14-25
G	Display Amp. Board	617-0017-00	12-13	14-27
H	ADC Board	617-0015-00	12-17	14-11
J	Trigger Board	617-0010-00	12-21	14-7
K	Offset Board	417-0024-00	12-21	14-5
L	Time Per Point Board	417-0025-00	12-21	14-5
M	Cursor Board	617-0018-00	12-22	14-7

320 ACCESSORIES

**TOP COVER**

ITEM	DESCRIPTION	ASSEMBLED BOARD	COMPONENTS	DIAGRAMS
A B	External Control Board Bubble Memory Assembly	SEE NOTE 1 222-0408-00	None	None

NOTE 1: The External Control Board is not available at this time.

MAIN ASSEMBLY

MAIN COMPONENTS			
ITEM	DESCRIPTION	PART NO.	QTY
01	Lid	042-902600	1
02	Plate	022-901701	1
03	See Table 2		
04	Top Cover	042-902500	1
05	Rail	034-901001	2
06	See Table 2		
07	Card Cage	033-900101	1
08	See Table 2		
09	Front Panel	068-905900	1
10	Latch	109-702100	2
11	See Table 2		
12	Plate	022-901504	1
13	Cushion	043-900000	2
14	Handle	049-900401	1
15	Cover	042-902400	1
16	Filter	114-900000	1
17	See Table 2		
18	CRT	027-700800	1
19	CRT Shield	044-904303	1
20	See Table 2		
21	See Table 2		
22	Switch	025-750900	1
23	Bottom Cover	042-903101	1
24	Fuse Holder	070-708800	1
25	Fan	072-702400	1
26	See Table 2		
27	Bumper	051-703600	4

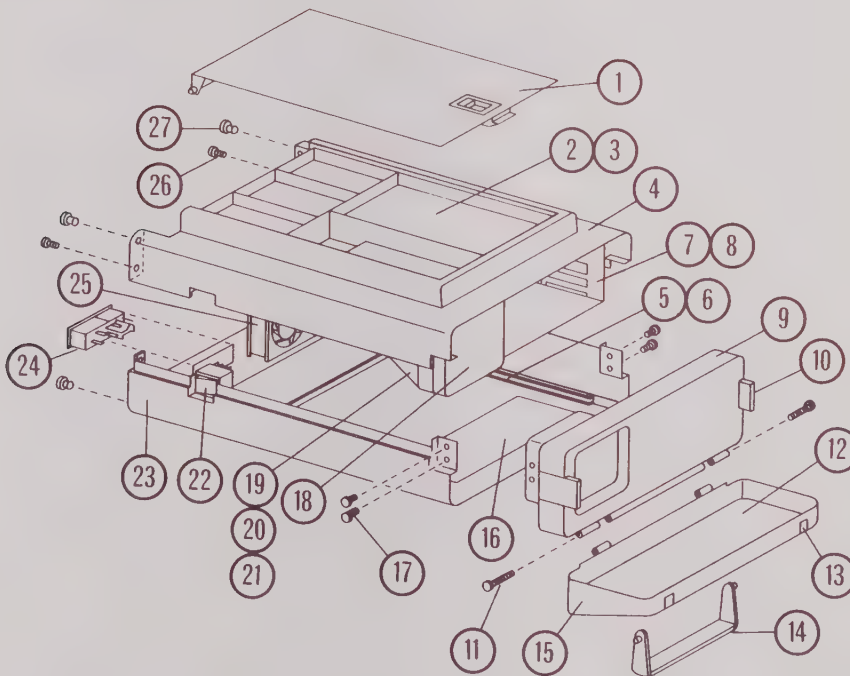
Table #1

HARDWARE		
ITEM	DESCRIPTION	QTY
03	440x0.250 CAP SO ST	4
06	632x0.250 CAP SO ST	4
08	632x0.250 CAP SO ST	4
11	832x2.125 CAP SO ST	2
18	440x0.250 FLT SO ST	4
20	160 Selfco Fastener	2
21	Split Retaining Ring	2
26	632x0.250 FLT SO ST	2

Table #2

320 PANEL OVERLAYS	
DESCRIPTION	PART NUMBER
Front Panel	068-905204
Rear Top Panel	068-904707
Rear Bottom Panel	068-905204

Table #3



320 REAR PANEL & BOTTOM COVER ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
1	477-002200	320 BOTTOM COVER ASSEMBLY	1.000
*2	617-001400	3XX REAR PANEL ASSEMBLY	1.000
**3	417-002600	3XX PEN POT ASSEMBLY	1.000
***4	000-915900	► PCB/300 PEN POT	1.000
***4	024-797300	CON 5M HDR/SOL S/RA AP	1.000
***4	026-900101	POT 250K PCB	1.000
**3	000-915800	► PCB/300 REAR PANEL	1.000
**3	023-702400	CAP .01MF 100V 20% CERM R SP	3.000
**3	023-722300	CAP .047MF 50V CERM G CL	1.000
**3	023-726400	CAP 4.7MF 10V 10% TANT R KE	1.000
**3	024-723200	CON 25M REC/SOL AMP 205737-1	1.000
**3	024-742200	CON 24F REC/SOL 552230-1 AM	1.000
**3	024-800500	CON 60M HDR/SOL 609-6024E TB	1.000
**3	024-900300	CON 1F CXL/SOL	3.000
**3	093-702100	FASTNER/SCR LOCK D20418-2 CI	2.000
**3	093-702700	FASTNER/CON/HWD 552633-4 AM	1.000
**3	134-756300	IC/555 DUAL 555 TIMER	1.000
**3	201-100100	RES 1K 01% 1/8W PRE	1.000
**3	201-100200	RES 10K 01% 1/8W PRE	2.000
**3	201-100300	RES 100K 01% 1/8W PRE	1.000
**3	260-1044005	STOF SWA 4-40X5/16 .250 SS	2.000
**3	260-1044007	STOF SWA 4-40X7/16 .250 SS	2.000
**3	260-1060004	STOF SWA #6 1/4 .250 SS	4.000
*2	017-716500	LABEL/3090 SERIAL NUMBER	1.000
*2	034-713300	GUIDE/SCANBE #11633-4	2.000
*2	034-901001	RAIL/3XX PROCESSOR BD.	2.000
*2	042-903101	COVER/3XX BOTTOM (EMI COATING	1.000
**3	042-902300	COVER/BOTTOM 3090	1.000
*2	051-703400	BUMPER 200-S BLACK LAV	2.000
*2	051-703600	BUMPER/5-44PB LA	2.000
*2	051-703700	BUMPER/PLUG 16-4PB LA	2.000
*2	051-703800	BUMPER/7/16"DIA BLK 827-S AI	2.000
*2	051-703900	BUMPER/ZB-1011 MR	2.000
*2	114-900000	FLTR/3090 AIR	1.000
*2	114-900101	FLTR/3XX AIR INTAKE	1.000
*2	002-901900	PLATE/3090 POWER SUPPLY GROUN	1.000
*2	025-750900	SW/RK 2PLIT 2-WIX11 DR	1.000
*2	060-703600	POST/BINDING 7/16" #110 HH	1.000
*2	068-905204	PAN/3XX REAR OVERLAY BOTTOM	1.000
*2	068-905205	PAN/3XX REAR OVERLAY BOTTOM	1.000
*2	070-708800	HOLDER/FUSE 42R38-3111-250 PD	1.000
*2	070-708801	HOLDER/FUSE 42R38-3111-150 PD	1.000
*2	085-905500	CBL 1 COND 2" LUG/LUG BROWN	1.000
*2	085-905600	CBL 1 COND 2" LUG/LUG BLUE	1.000
*2	085-905701	CBL 2 COND 3"/6" LUG/LUG/LVG	1.000
*2	113-707500	► PWR SPLY/5V +1-15 90W	1.000
*2	116-900400	SUPP/3XX REAR PANEL	1.000
1	011-905200	BRKT/3XX BUBBLE COVER	1.000
1	085-718300	PROBE/X1 COLINE 906-90-604	2.000

320 TOP COVER & HIGH VOLTAGE BOARD ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
1	477-002300	320 TOP COVER ASSEMBLY	1.000
*2	407-000600	3XX H.V. ANODE ASSY.	1.000
***3	015-718000	PIN F 16-28GA 02-08-110 TIN M	1.000
***3	024-712000	CON ANODE CT8 (BRIMAR)	1.000
*2	477-002400	3XX FAN ASSEMBLY	1.000
***3	024-779100	CON 2F SUP/IDP CE100F24-2 PD	1.000
***3	042-902700	COVER/FAN 3090	1.000
***3	072-702400	FAN/12V DC BRUSHLESS 3"	1.000
***3	078-710900	RING-0 .176ID .070W 568-00 LA	4.000
*2	617-000800	3XX HIGH VOLTAGE ASSEMBLY	1.000
***3	000-918500	PCB/300 HIGH VOLTAGE	1.000
***3	019-716400	INDUCT/SPE106 OPTION 0	2.000
***3	021-702200	TRN NPN 2N3903 40V 1W B MO	1.000
***3	021-706300	TRN PNP 2N3906 40V .625W B TX	2.000
***3	021-716200	TRN FETN IRFD110 100V 1W N IN	1.000
***3	022-700800	DIO RECT 1N4004 400V 1A G TX	10.000
***3	022-705100	DIO ZENR 1N5268 82V .5W G MO	1.000
***3	022-706900	DIO TRRF FM50 5KV .01A G SE	4.000
***3	022-707000	DIO TRRF S2F 200V 1A G SE	4.000
***3	022-713000	DIO RECT FDH300 150V .2A G FC	1.000
***3	022-715700	DIO ZENR 1N5246B 16V .5W G MO	1.000
***3	022-719800	DIO TRRF 1N4152 30V .5W G FC	2.000
***3	023-702400	CAP .01MF 100V 20% CERM R SP	1.000
***3	023-707300	CAP 1MF 200V 10% MYLR G TR	1.000
***3	023-711300	CAP .1MF 250V 10% PLYE R SE	2.000
***3	023-719400	CAP .01MF 3000V 20% CERM R SP	6.000
***3	023-721000	CAP 100MF 16V 20% TANT R IT	2.000
***3	023-722300	CAP .047MF 50V CERM G CL	1.000
***3	023-726300	CAP 22MF 35V TANT R KE	2.000
***3	023-726600	CAP 6.8MF 35V 10% TANT R KE	3.000
***3	023-728100	CAP .0047 6KV 20% CERM R	2.000
***3	023-732700	CAP .0022MF 100V 2% CERM KE	1.000
***3	026-712100	POT 10K PCB .5W 3299W1103 BR	1.000
***3	070-706000	FUSE/1A 256001 PICO II	1.000
***3	098-707200	HT SNK 6022B	1.000
***3	101-022500	RES 2.2M 10% 1/2W	1.000
***3	106-703600	RES 200M 10% 1W	1.000
***3	121-702100	REG 5 TO 30V 1A 78GU1C E FC	1.000
***3	134-711500	IC/555V TIMER T	1.000
***3	134-729403	IC/6N137	1.000
***3	201-100000	RES 100 01% 1/8W PRE	1.000
***3	201-100200	RES 10K 01% 1/8W PRE	2.000
***3	201-100300	RES 100K 01% 1/8W PRE	1.000
***3	201-100400	RES 1M 01% 1/8W PRE	1.000
***3	201-143000	RES 143 01% 1/8W PRE	1.000

320 TOP COVER & HIGH VOLTAGE BOARD ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
**3	201-150300	RES 150K 01% 1/8W PRE	1.000
**3	201-152200	RES 15.2K 01% 1/8W PRE	1.000
**3	201-162100	RES 1.62K 01% 1/8W PRE	1.000
**3	201-200200	RES 20K 01% 1/8W PRE	1.000
**3	201-200300	RES 200K 01% 1/8W PRE	1.000
**3	201-249000	RES 249 01% 1/8W PRE	1.000
**3	201-274000	RES 274 01% 1/8W PRE	1.000
**3	201-332000	RES 332 01% 1/8W PRE	3.000
**3	201-402300	RES 402K 01% 1/8W PRE	1.000
**3	201-499000	RES 499 01% 1/8W PRE	2.000
**3	201-511100	RES 5.11K 01% 1/8W PRE	1.000
**3	201-698100	RES 6.98K 01% 1/8W PRE	1.000
**3	201-887300	RES 887K 01% 1/8W PRE	1.000
**3	015-718100	PIN M .125 16-06-0005 TIN MOL	7.000
**3	019-900300	XFORMER/HIGH VOLTAGE 30XX	1.000
**3	067-700300	CORE/E1960-S-298A	2.000
**3	011-723103	BRKT/HI VOLT XFORMER/EXPL	1.000
**3	017-716600	LABEL/DANGER 6000 VOLTS	1.000
**3	G24-797100	CON 6F REC/SOL 09-52-3063 MO	1.000
**3	026-717600	POT 1MEG PML 1/2W 47-1M-S	2.000

320 TOP COVER & HIGH VOLTAGE BOARD ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
*2	002-901701	PLATE/3XX ADC COVER	1.000
*2	040-702600	CLIP/CABLE FCC-8-3 RP	2.000
*2	042-902600	COVER/TRAY 3090	1.000
*2	042-903002	COVER/3XX TOP (EMI COATING)	1.000
**3	042-902500	COVER/TOP 3090	1.000
*2	051-703600	BUMPER/5-44PB LA	2.000
*2	051-703900	BUMPER/ZB-1011 MR	2.000
*2	051-900502	BUMPER/300 SERIES TRAY #1	2.000
*2	051-900602	BUMPER/300 SERIES TRAY #2	1.000
*2	051-900700	PAD/FOAM 3XX TRAY #3	1.000
*2	066-900000	STRAP/3XX MANUAL 7.5"	1.000
*2	066-900100	STRAP/3XX MANUAL HOLD/DN 16.5	1.000
*2	066-900200	STRAP/3XX LINE CORD #1 4.1"	1.000
*2	066-900300	STRAP/3XX LINE CORD #2 5.375	1.000
*2	068-904707	PAN/3XX REAR OVERLAY TOP	1.000
*2	068-904708	PAN/3XX REAR OVERLAY TOP	1.000
*2	093-705700	FASTR/5/8" DIA BLK VELCRO H00	2.000
*2	109-702000	LATCH/3090 TOPCOVER A-3-40 SO	1.000
*2	017-901300	LABEL/3XX DISPLAY ADJUST	1.000
*2	017-901400	LABEL/3XX IO PARAMETER	1.000
*2	032-900200	INSUL/3XX BOTTOM COVER (FRONT	1.000
*2	032-900300	INSUL/3XX BOTTOM COVER (CENTE	1.000
*2	032-900400	INSUL/3XX BOTTOM COVER (STAND	2.000
*2	027-700800	CRT/140-DE831 5" CURVED FACE	1.000
*2	033-900101	CAGE/CARD 3XX SERIES	1.000
*2	044-904302	SHIELD/300 SERIES CRT	1.000
*2	044-904303	SHIELD/3XX CRT	1.000
*2	045-705200	KNOB/KU-4018 1/8 AL	1.000
*2	085-905802	CBL/1 COND 3" CRP/CRP AM	1.000
*2	093-705000	FASTNER/1/4 TURN PHILLIPS SO	2.000
*2	116-729000	SUPP/3090 CRT SHIELD SO	2.000
*2	116-900103	SUPP/3XX CRT FRONT	1.000
*2	243-100001	WSH SLK .222X.365X.015 S	2.000
*2	407-000500	300 SERIES CRT CABLE ASSEMBLY	1.000
**3	015-718000	PIN F 16-28GA 02-08-110 TIN M	11.000
**3	085-715800	CBL/12 COND CRT 622034-001	1.000

320 MOTHER BOARD & DISPLAY AMP BOARD ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
1	617-000600	320/DJ MOTHER BD. ASSEMBLY	1.000
*2	044-904800	SHIELD/3XX MOTHER BOARD	1.000
*2	617-001700	3XX DISPLAY AMP ASSEMBLY	1.000
**3	000-919300	► PCB/300 DISPLAY AMP	1.000
**3	023-722300	CAP .047MF 50V CERM G CL	8.000
**3	201-100000	RES 100 01% 1/8W PRE	6.000
**3	201-100100	RES 1K 01% 1/8W PRE	1.000
**3	201-130100	RES 1.3K 01% 1/8W PRE	1.000
**3	201-150100	RES 1.5K 01% 1/8W PRE	1.000
**3	201-162100	RES 1.62K 01% 1/8W PRE	2.000
**3	201-249100	RES 2.49K 01% 1/8W PRE	1.000
**3	201-316100	RES 3.16K 01% 1/8W PRE	1.000
**3	201-324200	RES 32.4K 01% 1/8W PRE	2.000
**3	201-453000	RES 453 01% 1/8W PRE	1.000
**3	201-499000	RES 499 01% 1/8W PRE	4.000
**3	201-499100	RES 4.99K 01% 1/8W PRE	3.000
**3	201-619100	RES 6.19K 01% 1/8W PRE	2.000
**3	201-681100	RES 6.81K 01% 1/8W PRE	2.000
**3	021-702200	TRN NPN 2N3903 40V 1W B MO	16.000
**3	021-711100	TRN NPN MPSU10 300V 1W E MO	8.000
**3	023-711300	CAP .1MF 250V 10% PLYE R SE	3.000
**3	023-716900	CAP 1.5 PFD ERIE	1.000
**3	023-717900	CAP 8PF 300V 6.2% MICA R AR	1.000
**3	023-726400	CAP 4.7MF 10V 10% TANT R KE	1.000
**3	024-799300	CON 34M HDR/SOL S/RA AP	1.000
**3	106-706900	RES 6.8K 2W 5% NON-IND CD	10.000
**3	201-750000	RES 750 01% 1/8W PRE	3.000
**3	023-700100	CAP 100PF 500V 05% MICA R AR	1.000

320 MOTHER BOARD & DISPLAY AMP BOARD ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
*2	000-915601	► PCB/3XX MOTHER	1.000
*2	015-718100	PIN M .125 16-06-0005 TIN MOL	6.000
*2	021-701800	TRN PNP 2N3905 40V .35W B MO	1.000
*2	021-702200	TRN NPN 2N3903 40V 1W B MO	1.000
*2	021-717500	FET IVN 6300 ANE	2.000
*2	022-719800	DIO TRRF 1N4152 30V .5W G FC	13.000
*2	023-707300	CAP 1MF 200V 10% MYLR G TR	1.000
*2	023-711200	CAP 220MF 10V 10% TANT G KE	1.000
*2	023-711300	CAP .1MF 250V 10% PLYE R SE	2.000
*2	023-722300	CAP .047MF 50V CERM G CL	15.000
*2	023-726400	CAP 4.7MF 10V 10% TANT R KE	9.000
*2	023-726600	CAP 6.8MF 35V 10% TANT R KE	18.000
*2	024-719500	CON 9M HDR/SOL AMP 9-350212-1	1.000
*2	024-779200	CON 2M HDR/SOL HLAS100-2 PN	1.000
*2	024-798000	CON 160M REC/SOL 532436-5 AM	1.000
*2	024-798100	CON 200M REC/SOL 532436-7 AM	1.000
*2	024-798300	CON 6M HDR/SOL 09-66-1061 MOL	1.000
*2	024-798400	CON 60M HDR-SOL D/ST AP	1.000
*2	024-798500	CON 26M HDR/SOL D/ST APT	1.000
*2	025-739700	SW/TH 1P1T08 76PSB08S GR	1.000
*2	025-741800	SW/TH 1P1T05 76PSB05S GR	1.000
*2	026-705300	POT 200 PCB .7W 3006P1201 BR	4.000
*2	026-705700	POT 5K PCB .7W 3006P1502 BR	2.000
*2	026-705800	POT 10K PCB .7W 3006P1103 BR	1.000
*2	026-706000	POT 20K PCB .7W 3006P1203 BR	3.000
*2	061-705500	LUG/62409-1 PC MOUNT AM	1.000
*2	121-702700	REG 5 TO 30V .5A 78MGU1C E FC	1.000
*2	121-702800	REG -2.2/-30V .5A 79MGU1C E FC	1.000
*2	121-703900	REG +12V .5A LM341P-12 E NA	1.000
*2	121-704800	REG -5V .1A 79L05 B T	1.000
*2	134-730603	IC/CA3140EX	1.000
*2	134-759400	IC/6012 DAC 12 BIT AM	2.000
*2	201-100100	RES 1K 01% 1/8W PRE	1.000
*2	201-100200	RES 10K 01% 1/8W PRE	4.000
*2	201-124000	RES 124 01% 1/8W PRE	1.000
*2	201-200100	RES 2K 01% 1/8W PRE	1.000
*2	201-221100	RES 2.21K 01% 1/8W PRE	1.000
*2	201-274100	RES 2.74K 01% 1/8W PRE	1.000
*2	201-324200	RES 32.4K 01% 1/8W PRE	1.000
*2	201-365000	RES 365 01% 1/8W PRE	1.000
*2	201-402000	RES 402 01% 1/8W PRE	2.000
*2	201-402200	RES 40.2K 01% 1/8W PRE	1.000
*2	201-412100	RES 4.12K 01% 1/8W PRE	1.000
*2	201-453200	RES 45.3K 01% 1/8W PRE	2.000
*2	201-499000	RES 499 01% 1/8W PRE	4.000
*2	201-499100	RES 4.99K 01% 1/8W PRE	3.000
*2	201-499200	RES 49.9K 01% 1/8W PRE	1.000
*2	201-523200	RES 52.3K 01% 1/8W PRE	1.000
*2	201-909100	RES 9.09K 01% 1/8W PRE	1.000
*2	024-798600	CON 50M HDR/SOL D/ST APT	1.000
*2	024-799600	CON 64F REC/SOL 543-416 ER	1.000
*2	046-704700	GRM/ID.375 00.438 LA	1.000

320 PROCESSOR BOARD ASSEMBLY

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
1	617-000700	320/370 PROCESSOR BD ASSY	1.000
*2	000-917900	► PCB/320/370 PROCESSOR	1.000
*2	134-712803	IC/74LS00N 2-NAND	4.000
*2	134-712903	IC/74LS04N HEX INVERTER	3.000
*2	134-756500	I/C LM358	1.000
*2	134-713203	IC/74LS74N FLIP-FLOP	2.000
*2	134-716103	IC/74S153N MULTIPLEXER	4.000
*2	134-719403	IC/74LS151N MULTIPLEXER	1.000
*2	134-719703	IC/7407N O/C HEX BUFFER	3.000
*2	134-720403	IC/74LS02N 2-NOR	1.000
*2	134-721203	IC/74LS163N COUNTER	4.000
*2	134-722703	IC/74LS08N 2-AND	3.000
*2	134-724903	IC/74S169 COUNTER	1.000
*2	134-732903	IC/74LS32N 2-OR	3.000
*2	134-736803	IC/74LS374N REGISTER	2.000
*2	134-739103	IC/74LS244N OCTAL BUFFER	4.000
*2	134-741703	IC/75188 QUAD LINE DRIVER	1.000
*2	134-769503	IC/74LS125 DIVER	1.000
*2	134-772503	IC/74ALS574 OCTAL D FLIP FLOP	4.000
*2	134-797200	I/C AD7528	1.000
*2	134-797300	I/C 400988	3.000
*2	134-798500	I/C PAL 16R8A-2	2.000
*2	134-798600	IC/PAL 16R4A-2	1.000
*2	134-806100	IC/4416-15 16KX4 DRAM 150NS	10.000
*2	134-797003	IC/74ALS1245 OCTAL BUFFER	7.000
*2	134-736803	IC/74LS374N REGISTER	3.000
*2	134-751800	IC/75161 488 BUFFER T	1.000
*2	134-777103	I/C 74ALS573	6.000
*2	134-801603	IC/74AS573 8BIT LATCH	2.000
*2	134-783903	IC/74LS166 SHIFT REGISTER	1.000
*2	134-739303	IC/74S139N DEMULTIPLEXER	1.000
*2	134-800000	IC/74ALS74 DUAL D FLIP FLOP	2.000
*2	134-710403	IC/74S00N 2-NAND	1.000
*2	134-756300	IC/556 DUAL 555 TIMER	1.000
*2	134-719503	IC/18S030 PROM (74S288)	1.000
*2	134-751700	IC/75160 488 BUFFER T	1.000
*2	134-715703	IC/74S04N HEX INVERTER	1.000
*2	013-701100	CONTACT/MALE CONTACT JUMPER	1.000
*2	021-702200	TRN NPN 2N3903 40V 1W 8 MO	2.000
*2	022-719800	DIO TRRF 1N4152 30V .5W 6 FC	4.000
*2	023-700400	CAP 47PF 500V 05% MICA R AR	3.000
*2	023-709100	CAP 20PF 500V 05% MICA R AR	2.000
*2	023-711300	CAP .1MF 250V 10% PLYE R SE	3.000
*2	023-722300	CAP .047MF 50V CERM G CL	40.000
*2	023-726400	CAP 4.7MF 10V 10% TANT R KE	15.000
*2	023-726600	CAP 6.8MF 35V 10% TANT R KE	3.000
*2	024-714700	CON 1M HDR/SOL CAS36SP100 CA	7.000
*2	024-724800	CON 40F DIP/SOL 641268-3 AM	1.000
*2	024-730900	CON 28F DIP/SOL 641267-3 AM	4.000
*2	024-738500	CON 1M HDR/SOL CAD72SP100 CA	40.000
*2	024-740700	CON 20F DIP/SOL 641264-3 AM	1.000
*2	024-789900	CON 48M REC/SOL EL	1.000

320 PROCESSOR BOARD ASSEMBLY

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
*2	024-790000	CON 200F REC/SOL 532903-7 AM	1.000
*2	024-799100	CON 68PIN L/L CARRIER TE	1.000
*2	024-799300	CON 34M HDR/SOL S/RA AP	1.000
*2	024-800600	CON 64M REC/SOL RA 533-606 ER	1.000
*2	025-739600	SW/PB 1P1TM MDP AU05 IE	1.000
*2	041-703600	XDUCER/AUDIO 6V SMX-06 ST	1.000
*2	085-906900	CBL 40 COND 14" DIP/HDR 3092	1.000
*2	100-700700	RES NET/CSP10E-01-502J	3.000
*2	100-704900	RES NET/DIP 270HM 16PN 8RES	2.000
*2	105-010000	RES 10 OHM 05% 2W	1.000
*2	121-702300	REG 1.2 TO 37V 1.5A 317T E NA	1.000
*2	121-703900	REG +12V .5A LM341P-12 E NA	1.000
*2	121-704000	REG -12V .5A LM79M12CP E NA	1.000
*2	133-900900	HYB/VECTOR DISPLAY INTERFACE	1.000
*2	134-752100	IC/9914 488 CONTROLLER T	1.000
*2	134-792000	IC/6264P-15/MB8464 8KX8 150NS	2.000
*2	134-797400	I/C 27128 250NS (16KX8) EPROM	4.000
*2	134-797500	I/C 80186-3 CPU 16BIT 8MHZ	1.000
*2	134-797700	IC/TMS 4500-15	1.000
*2	134-797900	I/C 8051	1.000
*2	191-711300	CRYS/7.3728MHZ .01% MPC18 NE	1.000
*2	191-711600	CRYS/OSC 32MHZ .01% HS100 NEL	1.000
*2	191-711700	CRYS/OC5 28MHZ .01% HS100 NEL	1.000
*2	201-100000	RES 100 01% 1/8W PRE	2.000
*2	201-100100	RES 1K 01% 1/8W PRE	6.000
*2	201-100200	RES 10K 01% 1/8W PRE	3.000
*2	201-100300	RES 100K 01% 1/8W PRE	2.000
*2	201-130100	RES 1.3K 01% 1/8W PRE	1.000
*2	201-137000	RES 137 01% 1/8W PRE	1.000
*2	201-150000	RES 150 01% 1/8W PRE	1.000
*2	201-162400	RES 1.62M 01% 1/8W PRE	1.000
*2	201-165200	RES 16.5K 01% 1/8W PRE	1.000
*2	201-249000	RES 249 01% 1/8W PRE	17.000
*2	201-274000	RES 274 01% 1/8W PRE	4.000
*2	201-324200	RES 32.4K 01% 1/8W PRE	1.000
*2	201-392000	RES 392 01% 1/8W PRE	1.000
*2	201-392900	RES 39.2 01% 1/8W PRE	2.000
*2	201-402100	RES 4.02K 01% 1/8W PRE	1.000
*2	201-453000	RES 453 01% 1/8W PRE	3.000
*2	201-475100	RES 4.75K 01% 1/8W PRE	4.000
*2	201-487000	RES 487 01% 1/8W PRE	1.000
*2	201-499100	RES 4.99K 01% 1/8W PRE	1.000
*2	201-499900	RES 49.9 01% 1/8W PRE	2.000
*2	201-698100	RES 6.98K 01% 1/8W PRE	1.000
*2	201-825900	RES 82.5 01% 1/8W PRE	1.000
*2	201-953900	RES 95.3 01% 1/8W PRE	5.000
*2	258-4040003	SPCR NT #4 X3/16 .187 AL	2.000
*2	049-704100	EJCTR/PCB 1/16"WHITE CP-46 BI	2.000
*2	105-010000	RES 10 OHM 05% 2W	1.000
*2	134-759800	IC/MK4802/HM6116-3 2K/8 150N	2.000
*2	201-010000	RES 10 01% 1/8W PRE	1.000
*2	201-100100	RES 1K 01% 1/8W PRE	3.000
*2	201-825900	RES 82.5 01% 1/8W PRE	1.000

320 ADC BOARD ASSEMBLY

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
1	617-001500	320 ADC ASSEMBLY	1.000
*2	032-700900	INSUL/DIODE	5.000
*2	000-918000	► PCB/320 ADC BD	1.000
*2	134-710403	IC/74S00N 2-NAND	1.000
*2	134-711203	IC/74S74N FLIP-FLOP	2.000
*2	134-763000	IC/OP-27GZ OPAMP	2.000
*2	134-713203	IC/74LS74N FLIP-FLOP	4.000
*2	134-716103	IC/74S153N MULTIPLEXER	1.000
*2	134-715703	IC/74S04N HEX INVERTER	1.000
*2	134-720403	IC/74LS02N 2-NOR	1.000
*2	134-720803	IC/74LS10N 3-NAND	1.000
*2	134-724903	IC/74S169 COUNTER	3.000
*2	134-723903	IC/74LS257 MULTIPLEXER	2.000
*2	134-731003	IC/74LS138N MULTIPLEXER	2.000
*2	134-732903	IC/74LS32N 2-OR	1.000
*2	134-738403	IC/F10125F ECL TRANSLATOR	7.000
*2	134-738903	IC/10124F ECL TRANSLATOR	1.000
*2	134-739003	IC/74S374N REGISTER	1.000
*2	134-739503	IC/74LS245 OCTAL TRANSCEIVER	3.000
*2	134-766703	IC/74F374 OCTAL FLIP FLOP	2.000
*2	134-772503	IC/74ALS574 OCTAL D FLIP FLOP	5.000
*2	134-793600	IC/11C70 ECL M/S D FLIP-FLOP	2.000
*2	134-794200	IC/CA3102B OP-AMP	2.000
*2	134-730903	IC/74LS367N HEX DRIVER	3.000
*2	022-713000	DIO RECT FDH300 150V .2A G FC	4.000
*2	022-714100	DIO SHT HSCH1001 60V15MAG HP	2.000
*2	022-719800	DIO TRRF 1N4152 30V .5W G FC	20.000
*2	023-722300	CAP .047MF 50V CERM G CL	55.000
*2	201-001000	RES 1 01% 1/8W PRE	6.000
*2	201-010000	RES 10 01% 1/8W PRE	14.000
*2	201-100000	RES 100 01% 1/8W PRE	29.000
*2	201-100100	RES 1K 01% 1/8W PRE	3.000
*2	201-100200	RES 10K 01% 1/8W PRE	1.000
*2	201-100400	RES 1M 01% 1/8W PRE	3.000
*2	201-124000	RES 124 01% 1/8W PRE	4.000
*2	201-137000	RES 137 01% 1/8W PRE	2.000
*2	201-140100	RES 1.4K 01% 1/8W PRE	2.000
*2	201-150100	RES 1.5K 01% 1/8W PRE	4.000
*2	201-187000	RES 187 1% 1/8W PRE	2.000
*2	201-200100	RES 2K 01% 1/8W PRE	4.000
*2	201-200200	RES 20K 01% 1/8W PRE	2.000

320 ADC BOARD ASSEMBLY

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
*2	201-205900	RES 20.5 01% 1/8W PREC	2.000
*2	201-221000	RES 221 01% 1/8W PRE	4.000
*2	201-232000	RES 232 01% 1/8W PRE	2.000
*2	201-249000	RES 249 01% 1/8W PRE	5.000
*2	201-249100	RES 2.49K 01% 1/8W PRE	2.000
*2	201-332000	RES 332 01% 1/8W PRE	3.000
*2	201-332100	RES 3.32K 01% 1/8W PRE	1.000
*2	201-357100	RES 3.57K 01% 1/8W PRE	2.000
*2	201-365000	RES 365 01% 1/8W PRE	2.000
*2	201-374100	RES 3.74K 01% 1/8W PRE	6.000
*2	201-392000	RES 392 01% 1/8W PRE	1.000
*2	201-402000	RES 402 01% 1/8W PRE	6.000
*2	201-412000	RES 412 1% 1/8W PRE	2.000
*2	201-412100	RES 4.12K 01% 1/8W PRE	1.000
*2	201-453000	RES 453 01% 1/8W PRE	2.000
*2	201-475100	RES 4.75K 01% 1/8W PRE	6.000
*2	201-475900	RES 47.5 01% 1/8W PRE	3.000
*2	201-499000	RES 499 01% 1/8W PRE	10.000
*2	201-499900	RES 49.9 01% 1/8W PRE	2.000
*2	201-562900	RES 56.2 01% 1/8W PRE	5.000
*2	201-619900	RES 61.9 01% 1/8W PRE	2.000
*2	201-681000	RES 681 01% 1/8W PRE	1.000
*2	201-681900	RES 68.1 01% 1/8W PRE	2.000
*2	201-715900	RES 71.5 01% 1/8W PRE	2.000
*2	201-750000	RES 750 01% 1/8W PRE	2.000
*2	201-825000	RES 825 01% 1/8W PRE	4.000
*2	019-718500	INDUCT/36.5NH CC	1.000
*2	019-900500	INDUCT/60NH	1.000
*2	021-702200	TRN NPN 2N3903 40V 1W B MO	1.000
*2	021-706300	TRN PNP 2N3906 40V .625W B TX	2.000
*2	021-710200	TRN NPN 2N5179 12V .2W A MO	16.000
*2	021-710700	TRN NPN A406 15V .5W A AM	9.000
*2	021-710800	TRN PNP A440 15V .2W A AM	4.000
*2	021-714000	TRN PNP MPS-H81 201 .35W B MO	11.000
*2	021-716100	TRN FETJN U440(M440) 25V 50MA	4.000
*2	022-700800	DIO RECT 1N4004 400V 1A G TX	4.000
*2	022-703700	DIO ZENR 1N5231 5.1V .5W G MO	2.000
*2	022-711600	DIO TRRF 1N4376 10V .05A G FC	14.000
*2	022-713000	DIO RECT FDH300 150V .2A G FC	4.000
*2	022-718500	DIO REF LM3368Z 2.5V	2.000
*2	022-719800	DIO TRRF 1N4152 30V .5W G FC	1.000
*2	022-723400	DIO BRID DMJ6575	2.000
*2	023-700100	CAP 100PF 500V 05% MICA R AR	10.000
*2	023-700300	CAP 500PF 500V 05% MICA R AR	2.000
*2	023-700500	CAP 250PF 500V 05% MICA R AR	2.000
*2	023-702400	CAP .01MF 100V 20% CERM R SP	18.000
*2	023-708800	CAP 33PF 500V 05% MICA R AR	2.000

320 ADC BOARD ASSEMBLY

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
*2	023-711300	CAP .1MF 250V 10% PLYE R SE	52.000
*2	023-715100	CAP .05MF 50V CERM R AR	4.000
*2	023-715500	CAP 1.5 TO .25PF TRIMMER R EF	4.000
*2	023-716900	CAP 1.5 PFD ERIE	3.000
*2	023-717900	CAP 8PF 300V 6.2% MICA R AR	2.000
*2	023-718800	CAP 4.7PF 500V CERM G ER	1.000
*2	023-722300	CAP .047MF 50V CERM G CL	5.000
*2	023-725600	CAP 5PF 300V 10% MICA R AR	4.000
*2	023-725900	CAP 3.5 TO 10PF 63V CERM ST	10.000
*2	023-726300	CAP 22MF 35V TANT R KE	8.000
*2	023-726400	CAP 4.7MF 10V 10% TANT R KE	48.000
*2	023-726600	CAP 6.8MF 35V 10% TANT R KE	9.000
*2	023-727300	CAP 7PF 300V MICA R AR	2.000
*2	023-727400	CAP 3.5 TO 10PF 63V CERM T ST	1.000
*2	023-733400	CAP 22PF 200V 10% CERM R KE	1.000
*2	023-735900	CAP 4T018 PF 250V TRIM JH	1.000
*2	024-724800	CON 40F DIP/SOL 641268-3 AM	1.000
*2	024-740700	CON 20F DIP/SOL 641264-3 AM	3.000
*2	024-796600	CON 32M REC/SOL G06D32P4BE CA	2.000
*2	024-796700	CON 160F REC/SOL 532434-5 AM	1.000
*2	026-710400	POT 100 PCB .5W 3299W1101 BR	2.000
*2	026-710700	POT 200 PCB .5W 3299W1201 BR	4.000
*2	026-712100	POT 10K PCB .5W 3299W1103 BR	2.000
*2	026-713200	POT 500 PCB .5W 3299W1501 BR	6.000
*2	067-701000	CORE/12-345-B PVLSE XFMR	2.000
*2	098-707200	HT SNK 6022B	5.000
*2	100-701900	RES NET/SIP 56 10PN 9RE	8.000
*2	100-702000	RES NET/SIP 560 10PN 9RE	2.000
*2	100-705700	RES NET/SIP 56 8 PN 7 RE	3.000
*2	100-705800	RES NET/SIP 4.7K 8PIN 7RES	3.000
*2	101-015100	RES 150 10% 1/2W	2.000
*2	121-702300	REG 1.2 TO 37V 1.5A 317T E NA	2.000
*2	121-702400	REG -1.2TO-37V 1.5A 337T E NA	4.000
*2	133-900700	HYB/3092 ATTENUATOR	4.000
*2	133-901000	HYB/GATE ARRAY 40MHZ XA COUNT	1.000
*2	134-739203	IC/74S32N 2-OR	1.000
*2	134-746700	IC/100131F ECL D FLIP FLOP	5.000
*2	134-746900	IC/100102F ECL 2INPUT OR/NOR	3.000
*2	134-793900	IC/8254-2 PROG COUNTER	2.000
*2	134-794000	IC/IMS1420-55 4KX4 55NS RAM	4.000
*2	134-798100	IC/7124H 512X8 PROM 35NS	3.000
*2	134-798200	IC/CX20052 8BIT 20MHZ ADC	2.000
*2	191-711400	CRYS/200 MHZ .0035% HC18 RH	1.000
*2	201-010000	RES 10 01% 1/8W PRE	2.000
*2	201-021900	RES 2.1 01% 1/8W PRE	4.000
*2	201-100000	RES 100 01% 1/8W PRE	2.000
*2	201-100100	RES 1K 01% 1/8W PRE	2.000

320 ADC BOARD ASSEMBLY

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
*2	201-178100	RES 1.78K 01% 1/8W PRE	2.000
*2	201-210900	RES 21 01% 1/8W PRE	2.000
*2	201-249100	RES 2.49K 01% 1/8W PRE	2.000
*2	201-267900	RES 26.7 01% 1/8W PRE	2.000
*2	201-332100	RES 3.32K 01% 1/8W PRE	1.000
*2	201-392000	RES 392 01% 1/8W PRE	1.000
*2	201-475100	RES 4.75K 01% 1/8W PRE	4.000
*2	201-487000	RES 487 01% 1/8W PRE	1.000
*2	201-499000	RES 499 01% 1/8W PRE	2.000
*2	201-562900	RES 56.2 01% 1/8W PRE	1.000
*2	201-750000	RES 750 01% 1/8W PRE	1.000
*2	201-909000	RES 909 01% 1/8W PRE	2.000
*2	023-709100	CAP 20PF 500V 05% MICA R AR	1.000
*2	024-798700	CON 1F JCK/SOL 8134-HC-8P AU	50.000
*2	025-900201	SW/RO 12POS5SEC S	2.000
*2	044-905900	SHIELD/320 ADC #1	1.000
*2	044-906000	SHIELD/320 ADC #4	1.000
*2	044-906100	SHIELD/320 ADC #3	1.000
*2	044-906200	SHIELD/320 ADC #2	1.000
*2	085-908100	CBL COAX 8" HDR/HDR 3092 ADC	2.000
*2	201-221000	RES 221 01% 1/8W PRE	1.000
*2	201-332000	RES 332 01% 1/8W PRE	3.000

320 DC OFFSET, TIME PER POINT, AND TRIGGER BOARD ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
1	667-000600	320 FRONT PANEL ASSEMBLY	1.000
**2	617-001000	320 TRIGGER ASSEMBLY	1.000
**3	417-002400	3XX DC OFFSET ASSEMBLY	1.000
****4	000-916900	▶ PCB/300 DC OFFSET	1.000
****4	023-722300	CAP .047MF 50V CERM G CL	6.000
****4	024-797200	CON 14M HDR/SOL D/RA AP	1.000
****4	026-900001	POT 1K/10K PCB	2.000
****4	134-730603	IC/CA3140EX	2.000
****4	201-100000	RES 100 01% 1/8W PRE	4.000
****4	201-249300	RES 249K 01% 1/8W PRE	2.000
**3	417-002500	3XX TIME/POINT ASSEMBLY	1.000
****4	000-916800	▶ PCB/300 TIME PER POINT	1.000
****4	024-797400	CON 6M HDR/SOL S/RA AP	1.000
****4	025-900402	SW/RO 1PL25PS 2035 SM PREL S	1.000
****4	201-100000	RES 100 01% 1/8W PRE	5.000
**3	000-918701	▶ PCB/320 TRIGGER	1.000
**3	134-743100	IC/SW7511FQ QUAD JFET SWITCH	1.000
**3	134-753700	IC/LM339 DIFFERENTIAL COMP.	1.000
**3	134-706600	IC/LM301 OPAMP NA	1.000
**3	134-727600	IC/1458 OPAMP	1.000
**3	134-773400	IC/10102L ECL GATE	1.000
**3	134-794400	IC/AM6850L COMPARATOR	1.000
**3	022-713000	DIO RECT FDH300 150V .2A G FC	2.000
**3	022-719800	DIO TRRF 1N4152 30V .5W G FC	9.000
**3	023-722300	CAP .047MF 50V CERM G CL	19.000
**3	201-100000	RES 100 01% 1/8W PRE	8.000
**3	201-100100	RES 1K 01% 1/8W PRE	2.000
**3	201-100200	RES 10K 01% 1/8W PRE	10.000
**3	201-100400	RES 1M 01% 1/8W PRE	2.000
**3	201-105200	RES 10.5K 01% 1/8W PRE	1.000
**3	201-124000	RES 124 01% 1/8W PRE	1.000
**3	201-124200	RES 12.4K 01% 1/8W PRE	2.000
**3	201-130100	RES 1.3K 01% 1/8W PRE	1.000
**3	201-150100	RES 1.5K 01% 1/8W PRE	1.000
**3	201-158200	RES 15.8K 01% 1/8W PRE	1.000
**3	201-165200	RES 16.5K 01% 1/8W PRE	1.000
**3	201-178000	RES 178 01% 1/8W PRE	1.000
**3	201-178200	RES 17.8K 01% 1/8W PRE	2.000
**3	201-200100	RES 2K 01% 1/8W PRE	1.000
**3	201-221000	RES 221 01% 1/8W PRE	1.000
**3	201-237100	RES 2.37K 01% 1/8W PRE	2.000
**3	201-249000	RES 249 01% 1/8W PRE	1.000
**3	201-249300	RES 249K 01% 1/8W PRE	1.000
**3	201-274100	RES 2.74K 01% 1/8W PRE	4.000
**3	201-324200	RES 32.4K 01% 1/8W PRE	1.000

320 TRIGGER BOARD AND CURSOR BOARD ASSEMBLIES

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
**3	201-402100	RES 4.02K 01% 1/8W PRE	2.000
**3	201-499900	RES 49.9 01% 1/8W PRE	3.000
**3	201-511100	RES 5.11K 01% 1/8W PRE	1.000
**3	201-562000	RES 562 01% 1/8W PRE	2.000
**3	201-649000	RES 649 01% 1/8W PRE	1.000
**3	201-750100	RES 7.5K 01% 1/8W PRE	1.000
**3	201-806300	RES 806K 01% 1/8W PRE	1.000
**3	201-825900	RES 82.5 01% 1/8W PRE	1.000
**3	201-909100	RES 9.09K 01% 1/8W PRE	1.000
**3	021-714000	TRN PNP MPS-H81 201 .35W B MO	2.000
**3	021-716100	TRN FETJN U440(M440) 25V 50MA	1.000
**3	022-700800	DIO RECT 1N4004 400V 1A G TX	3.000
**3	022-711600	DIO TRRF 1N4376 10V .05A G FC	1.000
**3	023-700300	CAP 500PF 500V 05% MICA R AR	1.000
**3	023-700400	CAP 47PF 500V 05% MICA R AR	1.000
**3	023-706800	CAP 150PF 500V 05% MICA R AR	1.000
**3	023-709100	CAP 20PF 500V 05% MICA R AR	1.000
**3	023-711300	CAP .1MF 250V 10% PLYE R SE	4.000
**3	023-711800	CAP .001MF 200V 10% PLYE G SP	1.000
**3	023-722300	CAP .047MF 50V CERM G CL	1.000
**3	023-726400	CAP 4.7MF 10V 10% TANT R KE	6.000
**3	023-726600	CAP 6.8MF 35V 10% TANT R KE	2.000
**3	024-714700	CON 1M HDR/SOL CAS36SP100 CA	4.000
**3	024-796500	CON 32F REC/SOL G06D32P3BD CA	1.000
**3	098-707200	HT SNK 6022B	2.000
**3	100-705700	RES NET/SIP 56 8 PN 7 RE	1.000
**3	121-702300	REG 1.2 TO 37V 1.5A 317T E NA	1.000
**3	121-702400	REG -1.2TO-37V 1.5A 337T E NA	1.000
**3	134-711900	IC/LM318H OPAMP	1.000
**3	201-100200	RES 10K 01% 1/8W PRE	1.000
**3	024-764200	CON 1F HDR/SOL 026-1800 SEL	1.000
**3	024-900300	CON 1F CXL/SOL	3.000
**3	025-751100	SW/T0 2PL ON-ON-ON B24KP NK	3.000
**3	025-751200	SW/T0 2PL ON-OFF-ON B23KP NK	1.000
**3	025-751300	SW/T0 2PL ON-ON B22KP/407 NK	2.000
**3	026-708000	POT 2K PCB .5W 3299W1202 BR	2.000
**3	026-900302	POT 25K PCB	1.000
**3	201-100400	RES 1M 01% 1/8W PRE	1.000
*2	617-001800	➤ 3XX CURSOR ASSEMBLY	1.000
**3	000-916200	PCB/300 CURSOR	1.000
**3	022-723700	DIO DUAL 8AW56 70V .1A SOT23	16.000
**3	022-724600	DIO/LEDG HLMP2500 H	7.000
**3	022-724700	DIO/LEDY HLMP2400 H	5.000
**3	022-724800	DIO/LEDR HLMP2300 H	3.000
**3	022-724900	DIO/LEDR HLMP2350 H	2.000
**3	024-796500	CON 32F REC/SOL G06D32P3BD CA	1.000
**3	024-797900	CON 48F REC/UWP 00-8257-04 EL	1.000
**3	200-150000	RES 150 1% 1/8W	7.000
**3	200-182000	RES 182 01% 1/8W	5.000
**3	200-274000	RES 274 01% 1/8W	7.000

320 FRONT PANEL ASSEMBLY

RELATIVE LEVEL	COMPONENT PART NO.	DESCRIPTION (Truncated)	QTY (Each)
*2	002-901503	PLATE/300 SERIES FRONT COVER	1.000
*2	002-901504	PLATE/3XX COVER	1.000
*2	011-904000	BRKT/300 SERIES COVER PLATE	2.000
*2	011-904600	BRKT/3XX RETAINER	2.000
*2	011-904700	BRKT/3XX HANDLE ASSEMBLY	2.000
*2	015-900001	PIN/3XX HANDLE	2.000
*2	042-902400	COVER/FRONT PANEL 3090	1.000
*2	043-900000	STRIP/FRONT RUBBER 3XX	2.000
*2	049-900401	HANDLE/300 SERIES	1.000
*2	243-060002	WSH SLK/RETAINING RING S	2.000
*2	017-901000	LABEL/320 MODEL NUMBER	1.000
*2	035-704800	BUTT/AT467K BLACK .370" NK	6.000
*2	035-900004	BUTT/300 FRONT PANEL PUSH	1.000
*2	035-900100	BUTT/3XX FRONT PANEL SEC.#1	1.000
*2	035-900200	BUTT/3XX FRONT PANEL SEC.#2	1.000
*2	044-905700	SHIELD/3XX CURSOR	1.000
*2	044-905800	SHIELD/320 TRIGGER	1.000
*2	045-900500	KNOB/3090 3010-10	2.000
*2	045-900600	KNOB/3090 3009-10	1.000
*2	045-900700	KNOB/3090 3008-10	1.000
*2	045-900800	KNOB/3090 3008 EH	2.000
*2	068-904805	PAN/320 FRONT OVERLAY	1.000
*2	068-906802	PAN/3XX FRONT (EMI COATING)	1.000
**3	068-905900	PAN/3090 FRONT	1.000
*2	109-702100	LATCH/HINGE DRAW 07-10-205 SO	2.000
*2	164-900102	GRAT/300 SERIES	1.000
*2	164-900200	GRAT/320 CRT	1.000
*2	230-083234	SCR 8-32X2.125 CAP SO ST B	2.000
1	085-906400	CBL 60 COND 6" HDR/HDR 3090	1.000
1	085-906700	CBL 20 COND 4" HDR/HDR 3090	1.000
1	042-901903	PLATE/3XX COVER/REMOTE CONTR	1.000
1	042-902202	PLATE/3XX COVER/BUBBLE	1.000
1	085-725800	CORD/A/C/LINE 17745 BE	1.000

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320 CPU DESCRIPTION

THE MAIN PROCESSOR

The main processor on this board is the Intel 80186, a 16 bit device with a multiplexed address/data bus.

Twenty address lines are available from the device to allow addressing of up to 1 mega-byte of memory space. The address bus is de-multiplexed from the address/data bus using two 74ALS573's and the control signal ALE'.

The 16 bit data bus is made by buffering the address/data bus with two 74ALS1245 bidirectional drivers controlled by the signals DEN- and DT/R-. DEN- goes true during memory and I/O accesses while DT/R- controls the direction of the data flow.

The 80186 is a highly integrated device that includes the memory and peripheral chip selects, timers, interrupt controller, DMA controller, wait state generator, etc. A bank of control registers located within the 80186 is used to control the operation of these internal devices.

There are 6 memory chip selects and 7 peripheral chip selects available on the 80186.

#1. Memory Chip Selects

MCS0- - Selects the on-board static RAM area where interrupt vectors, user variables, stack, etc. will reside.

UCS- - Selects the program memory area that will be occupied by either EPROMs or masked ROMs.

There are four mid-range chip selects that are used to select other memory areas:

a. MCS2-, MCS3-

Selects the 32K word display memory area. Each signal selects a 16K word bank of memory.

b. MCS1-

Selects the 16K word data memory area which will be used for waveform data storage.

#2. Peripheral Chip Selects

The 7 peripheral chip selects are active for seven continuous blocks of 128 bytes above a programmable base address. This base address is located in the I/O space.

CS8051- -- Selects the interface to the 8051 processor.

PI1EN- --- Used to select the ADC interface.

PI2EN- --- Not used.

PI3EN- --- Not used.

CSLED- --- This signal selects the discrete LED drivers and the 7-segment LED drivers. It is also used as a general purpose latch signal to clock on board registers when combined with the appropriate address line.

CS488- --- Selects the IEEE-488 remote control interface.

CSBM- ---- Selects the bubble memory interface.

All of the preceding memory and peripheral chip selects must be programmed via the internal control registers at power up to function properly. Wait states can also be programmed for those memory or peripheral chip selects that require longer access.

THE DATA MEMORY

The data memory consists of four TMS4416-15 16K x 4 DRAM ICs and one TMS4500A DRAM controller. 16K words can be accessed when all four memory ICs are loaded.

The 4500A interfaces the memory to the 80186 and handles all of the critical timing. The data memory area is selected via MCS1-. One wait state is required when accessing the data memory and this is accomplished by strapping 4500A inputs FS1, FS0, and TWST appropriately. Waveform data will be stored in this area.

THE STATIC RAM

The processor's internal static RAM is byte addressable.

Interrupt vectors, user variables, stack, etc., reside in this area and are selected via MCS0-.

THE DISPLAY MEMORY

The display memory consists of 32K words that are split into two banks of 16K words with the low bank being selected with MCS2- and the high bank with MCS3-. The display memory is controlled by a state machine that is asynchronous to the 80186.

Information contained in the memory consists of all the dot information displayed on the CRT along with control information for controlling features of the display.

Since the display memory runs asynchronous to the 80186, the 80186 must make a memory request to the memory controller in order to read from or write into the memory. The controller will accept the request, generate a hardware wait condition to the 80186, and then honor the request when a time slot becomes available in the display memory timing sequence.

When the memory access has been completed, the controller will release the hardware wait condition to allow the 80186 to complete its' memory cycle.

8051 PROCESSOR INTERFACE

The 8051 processor is used to relieve the 80186 from all front panel tasks.

Secondary tasks of the 8051 are:

1. To act as the serial data port for all serial transfers into and out of the instrument.
2. Holds the X,Y dot information for the character set and transfers this information to the 80186 upon request.

Communication between the two processors is done via an 8-bit bi-directional latched port, plus status and interrupt lines.

- a. When the 8051 wants to talk to the 80186, it interrupts the 80186.
- b. When the 80186 reads the data, it will interrupt the 8051 to complete the handshake.
- c. When the 80186 wants to talk to the 8051 it interrupts the 8051 and sends out a byte of data. If additional information is required, the 80186 will monitor a status line and when the 8051 has read the first byte the 80186 will send the next byte.

#1. Front Panel Task

The 8051 program controls a group of 8 strobe lines that goes to all push-buttons, switches, etc., in order to enable reading the switch contacts to determine whether the contacts are open or closed. The result of the readings are returned to the processor via a group of 8 return lines, RET0-RET7.

The information about the state of the switches is stored in RAM memory of the 8051. When a change in switch state is detected, the switch is debounced, the internal memory is updated, and the 80186 is notified that the switch changed state. The 80186 then will determine whether the state change was of consequence or not. Thus, the 80186 contains the intelligence associated with all of the switches, buttons, etc.

#2. Serial Data Tasks

The 8051 has serial port capability integrated on chip and therefore serves as the serial interface in the 320. All serial information (received or transmitted) is passed through the 8051. A buffer area is set up in the internal RAM of the 8051 to hold serial data that is received. This data will be passed on to the 80186 as the interface allows. On data transmission the 80186 transfers data to the 8051 which then formats the data and sends it out the serial port. When transmission is complete the 8051 informs the 80186 that it is ready to transmit more data.

#3. Character Data Task

The character information for the characters displayed by the 320 is stored in ROM on the 8051. The character data is stored in the form of X,Y pairs where each X,Y pair represents a single dot on the display.

The 80186 requests a character by sending the ASCII character representation to the 8051. The 8051 uses the ASCII representation as an index into the ROM area where the X,Y pairs for that particular character are stored.

The 8051 sends the X-coordinate and then the Y-coordinate back to the 80186. The 80186 then requests additional X,Y pairs until all of the character data has been transferred.

NOTE: See the device description for the 8051/80186 interface (starting on page 13-23) for additional information about data transfers between the two processors.

THE BUBBLE MEMORY INTERFACE

The bubble memory interface, selected by CSBM-, consists of an 8 bit bi-directional buffer for the data lines and a few combinational logic gates to generate read and write signals to the bubble memory.

Address lines A1, A2, and A3 are used to address 8 read/write registers in the bubble memory controller. All communication with the bubble memory is accomplished by setting up these registers with the appropriate information. Combinational logic is used to delay the bubble memory read and write signals from the processor read and write signals to accommodate timing restrictions imposed by the

bubble memory controller. The 8 data lines reside on the upper 8 data lines of the processor bus. This was done to help distribute the loading of the processor data bus. The bubble memory has DMA capability and the ability to interrupt the processor when service is required. At the present time, however, these features are not used but the appropriate signals are available on the processor board for possible future use. One wait state is required when accessing this interface.

IEEE-488 REMOTE CONTROL INTERFACE

The remote control interface consists of an TMS9914A controller chip and two bus transceiver chips that are required to make the IEEE-488 bus conform to the standard. In all appearances, the interface is similar to the bubble memory interface.

Three address lines, A1-A3, a read line and a write line are used to communicate with the control registers located within the IEEE-488 controller chip. Data is transferred via 8 bidirectional data lines which reside on the lower 8 bits of the processor data bus.

Signal CS488- selects the IEEE-488 interface. Communication with the 80186 is interrupt driven with the controller chip interrupting the 80186 when it requires service. DMA capability is provided but is not used at the present time. One wait state is required when accessing this interface.

LED DRIVER INTERFACE

The LED driver interface for the 320 consists of a 16 bit write only latch, open collector driver gates, and a few miscellaneous logic gates to generate the appropriate control signals. This arrangement allows for driving 16 discrete LEDs. Selection is accomplished with CSLED- and address line A1. The board also includes room to insert an Intersil 7218A 7-segment LED driver IC. This was included for future use as the outputs are not currently available on any of the PC board connectors. Selection of this IC is done with CSLED- and address line A2.

MOTHER BOARD INTERFACE

In order to allow external devices (such as the ADC) to interface to the processor board, the address lines, data lines, and appropriate control lines are buffered and run off board on the J15 connector.

PI1EN-, -- The three peripheral
PI2EN-, selects that run off
PI3EN- board.

Bidirectional drivers are used to buffer all of the address and data lines that go off the processor board and control circuitry was added to keep these lines inactive unless the appropriate peripheral select or memory select is active.

There are three input signals brought on board and buffered at the J15 connector.

PIINT1-, -- These two are interrupt
PIINT2- lines that may be driven by the external device when requesting service from the 80186.

DRQ1- ----- This is the DMA request line to the 80186. It is used by the external devices that need DMA capability.

The above three signals also have pull-up resistors to +5 volts to keep them inactive when not in use.

PEN OUTPUT INTERFACE

The pen output interface consists of an AD7528 dual 8 bit DAC and two OP AMPS to drive the pen X and Y outputs. The 8 data lines reside in the upper 8 bits of the processor (for distribution purposes) and the interface is selected with CSLED- and address line A3. Address line A4 controls selection of the two DACs.

REGULATORS

Two +12V and two -12V regulators are used on board to supply voltages required by the bubble memory, DACs, display circuitry, LEDs, etc.

PROCESSOR CLOCK CIRCUITRY

A 32 MHz crystal oscillator output is divided by 2 and by 4 to provide the clock inputs for the 80186 and the state machine that controls the display.

The 80186 internally divides its 16 MHz clock input by 2 to generate an 8 MHz clock that runs the processor. This 8 MHz clock is available out of the processor and is used in several places on the board to synchronize circuitry to the processor. The 16 MHz and 8 MHz signals from the divider are used to clock the state machine for display circuitry.

320 ADC CONTROLLER

The 320 ADC board to 320 Processor board interface contains:

- #1. A 16-bit data bus (PD0-PD15) used to write (or read) information into (or out of) several on-board registers. The data bus is buffered.
- #2. An I/O Read Control line (RDMB-).
- #3. An I/O Write Control line (WRMB-).
- #4. Three least significant address lines (ADMB1, ADMB2, ADMB3) used to select which of the registers will be written into (or read from). In addition, address lines 5 and 6 select registers within the Dwell Counter and Delay Counter.
- #5. An I/O Chip Select line (PI1EN-).

- #6. An ADC Controller Interrupt (PIINT0) line.

NOTE: The processor board cannot directly access an ADC memory location. All data transfers out of the ADC's memory have to be accomplished through a register.

The 320 ADC Board resides in the processor's I/O space and is enabled by the signal "PI1EN-" connected to the "PCS1-" line of the processor. This means that the 320 ADC's eight registers reside at I/O space locations 0080H through 008EH.

Table 13-1 tabulates the eight read-only registers and write-only registers that reside on the controller. Detailed descriptions of each register begins on page 13-14.

I/O LOCATION	READ REGISTERS (IORD- = 0)	WRITE REGISTERS (IOWR- = 0)
0080H	ADC Data	Cursor Trigger Locations
0082H, 00A2H, 00C2H, 00E2H	Dwell Counter	Dwell Counter
0084H	Not Used	Command
0086H	Status	Not Used
0088H, 00A8H, 00C8H, 00E8H	Delay Counter	Delay Counter
008AH, 008CH, 008EH	Not Used	Not Used

Table 13-1

**ADC DATA REGISTER
(Read Only - Location 0080H)**

When the ADC Controller finishes collecting data, it sends a Processor interrupt signal "ADC-INT" to the Processor board.

When an interrupt occurs, the ADC controller's memory pointer (SA0 - SA11) points at the address containing the data to be transferred to the processor. Which address will be pointed at is determined by whether the 320 is in the Fast or Slow mode.

Fast Mode (Burst Dump)

The pointer points at the address containing the data point to be displayed on the right-hand side of the screen. The ADC controller automatically decrements the memory address when the processor reads this first data point.

Slow Mode (Nonburst Dump)

The pointer points at the address containing the data point that was just digitized.

NOTE: The processor always reads data from channel A first, and then Channel B every time it reads data from the ADC controller. The 8-bit data field is left justified on the 16-bit data bus. The data is represented as a two's complement number and the memory length is 4000 words per channel.

DWELL COUNTER REGISTER**Read and Write****(Locations 0082H, 00A2H, 00C2H, 00E2H)**

The Dwell Counter is an Intel 8245-2, which contains three 16-bit counters (locations 0082H, 00A2H, and 00C2H) and one command register (location 00E2H). The four internal registers are selected by address lines 5 and 6. It's input is 8-bits wide and it is on the least significant byte of the 16-bit bus.

In general, the DWELL COUNTER will be a write-only device, but the ADC controller also allows the processor to read the status register and the count value of any particular counter.

A. Command Register (Location 00E2H)

In order to initiate a count the processor writes a control word to the command register. This control word identifies which counter will be loaded and in which mode it is to operate.

B. Counter 0 (Location 0082H)

Counter 0 generates the AUTO TRIG pulse.

AUTO TRIG is turned on by setting counter 0 to mode 2 and loading a large count value.

AUTO TRIG is turned off by setting counter 0 to mode 2, and not giving it a count. This disables the count output.

C. Counters 1 & 2 (00A2H and 00C2H)

Counter 1 and Counter 2 are cascaded to form a 32-bit counter.

Counter 1 has the least significant 16 bits and Counter 2 has the most significant 16 bits.

NOTE: If the 320 ADC only needs a small count (Time Per Point is 1mS or less), COUNTER 2 can be disabled (output low) by initiating it to mode 0 and not giving it a count value.

Table 13-2 shows the Time Per Point setting and the associated count values for Counter 1 and Counter 2.

DWELL COUNTER TABLE		
TIME PER POINT	COUNTER 1	COUNTER 2
5 nS	1	0
10	1	0
20	1	0
50	1	0
100	1	0
200	2	0
500	5	0
1 μ S	10	0
2	20	0
5	50	0
10	100	0
20	200	0
50	500	0
.1 mS	1000	0
.2	2000	0
.5	5000	0
1	100	100
2	200	100
5	500	100
10	1000	100
20	2000	100
50	5000	100
100	100	10000
200	200	10000
500	500	10000

Table 13-2

STATUS REGISTER
Read only (Location 0086H)

The Status Register is right justified on the 16-bit processor bus. Figure 13-1 indicates the contents of the status register.

AOR5 - AOR0 - The Address Offset Return indicates the relative time difference of the trigger pulse and the sample pulse. This is only used when the 320 is in sampling mode (5nS to 50nS). The information is used by the processor to determine into which display memory address the ADC data will be written.

PTRIG --- This flag goes high after a trigger is recognized.

SWPDONE - This flag goes high when the ADC controller has finished an entire sweep. A sweep constitutes 4000 points in the non-sampling mode and either 2000, 800, 400, or 200 points in the sampling mode.

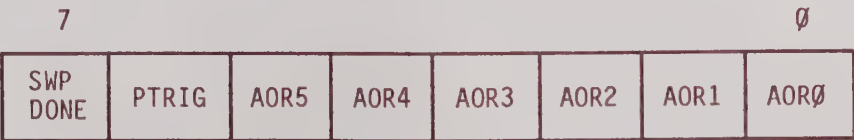


Figure 13-1

CURSOR TRIGGER LOCATION REGISTER
Write Only (Location 0080H)

The processor's Cursor Trigger Location register records the position of the cursor trigger. If the 320 is in the normal trigger mode, a 0000 will be written into the register. This register is contained within the XA counter IC.

NOTE: Data written into the cursor trigger register is in BCD format.

When the 320 is in the non-sampling mode (4000 pts), the cursor trigger register can range from 0 to 3999 decimal.

If the 320 is in the sampling mode (e.g., Time Per Point = 10nS), it will need 10 sweeps of 400 points each to fill the 4000 word data memory. The cursor trigger register will then have a range of 0 to 399 decimal. In other words, the processor cannot load the Cursor Trigger Register with a number larger than the number of points in the sweep.

COMMAND REGISTER**Write Only (Location 0084H)**

The command register performs seven different functions. Five of these functions are set during the initialization of the controller between sweeps. The sixth function is the "go" bit (called RESET), and the seventh function is a Power-Up bit which is used to synchronize the clocks.

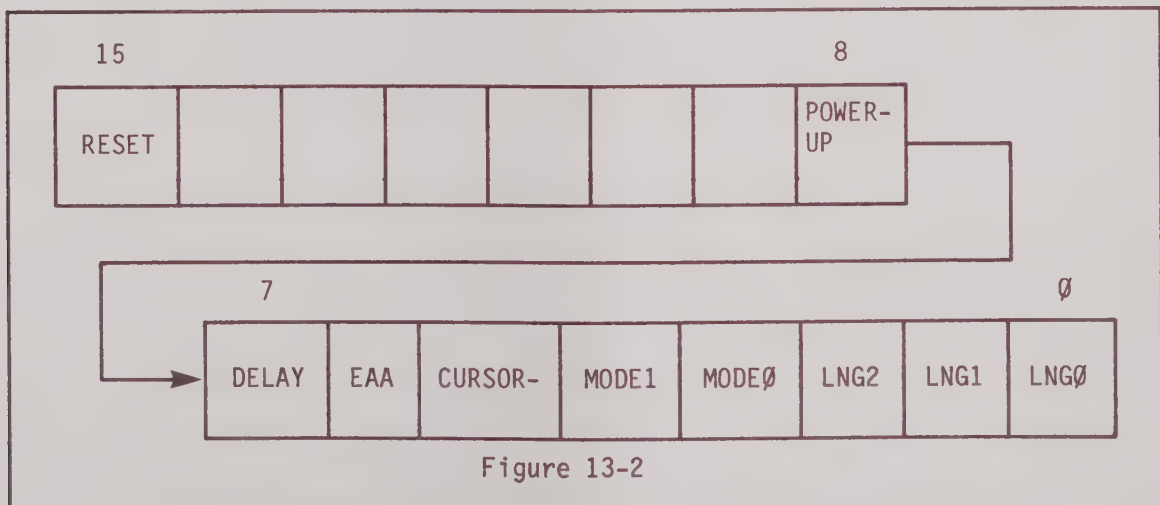
Figure 13-2 describes the functions of the 16-bit command register.

RESET - When Reset is high, the ADC controller's state machine returns to its' initial state and remains there. When Reset is low, the controller starts a new sweep.

NOTE: No other command register transitions can occur while the Reset bit is changed.

DELAY - The DELAY bit enables the delay trigger counter.

EAA --- When high, the External Address Advance bit allows the ADC board to get its dwell pulses from the EAA input.



COMMAND REGISTER continued

CURSOR- - When low, the Cursor Trigger bit sets the control board to the cursor trigger mode. The cursor trigger register has to be loaded appropriately.

MODE1, -- These bits set the mode of
MODE0 --- operation of the controller to Table 13-3.

MODE1	MODE0	MODE	TIME PER POINT
0	0	FAST	200nS - 20μS
0	1	100nS	100nS
1	0	SLOW	50μS - 1 sec
1	1	SAMPLE	5nS - 50nS

Table 13-3

NOTE: In the SLOW mode, the ADC controller dumps data in the non-burst mode. In all other modes (100nS, FAST, SAMPLING) the controller will dump data in the burst mode.

LNG2 - LNG0 - The Length 2, Length 1, and Length 0 bits pick the memory length of the ADC board. Table 13-4 describes how these bits are decoded. These bits are accessible on the command register although they are decoded internally to the XA counter IC.

LNG 2	LNG 1	LNG 0	MEMORY LENGTH (Decimal)
0	0	0	100
0	0	1	200
0	1	0	400
0	1	1	800
1	0	0	1000
1	0	1	2000
1	1	0	4000
1	1	1	8000

Table 13-4

DELAY COUNTER REGISTER**Read and Write****(Locations 0088H, 00A8H, 00C8H, 00E8H)**

The Delay Counter (an Intel 8254-2) contains three 16-bit counters (Locations 0088H, 00A8H, and 00C8H) and one Command Register (Location 00E8H). The four internal registers are selected by address lines 5 and 6. It's input is 8-bits wide and on the least significant byte of the 16-bit bus.

Counter 0 (least significant bit) and Counter 1 (most significant bit) are run in Mode 4. Counter 2 is not used.

NOTE: The resolution of the delay counter is limited to 1 μ s intervals. The maximum delay allowed is 400 seconds.

The Delay Counter works in conjunction with the DELAY bit of the Command Register (00E4H). The amount of delay is determined by the counter while the initiation of TRIGGER DELAY is done by setting the DELAY bit in the Command Register.

Flow chart 13-1 (page 13-22) describes how the software determines the values that have to be loaded into the least significant bit Delay Counter (Counter 0) and the most significant bit Delay Counter (Counter 1).

DELAY COUNTER VALUES FLOW CHART

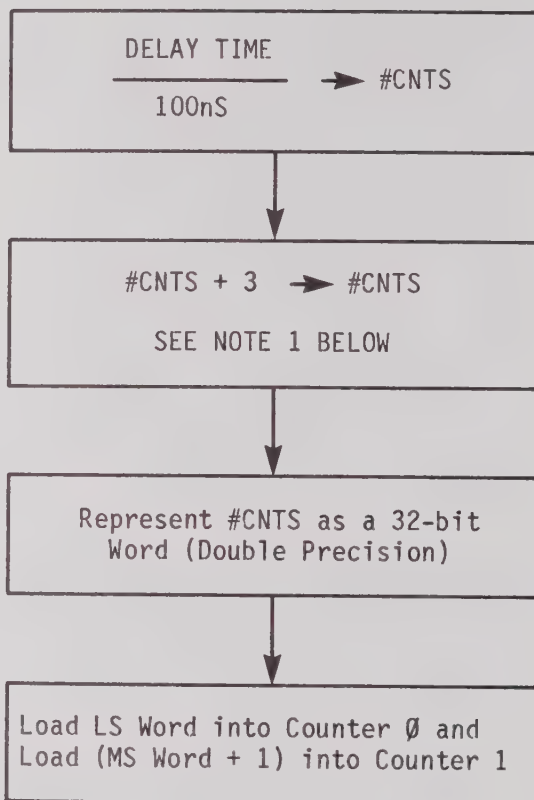
INPUT -- Desired delay time (1 μ S to 400S)

OUTPUT - Least significant counter's initial value and the most significant counter's value

OPERATING THE ADC CONTROLLER

To operate the ADC controller, the processor performs the following operations:

- #1. Load the DWELL COUNTER
- #2. Load the CURSOR REGISTER or the DELAY REGISTER.
- #3. Load the COMMAND REGISTER.
- #4. Disable the RESET bit.
- #5. Respond to the interrupt that will be generated at the end of the sweep.
- #6. Check the STATUS REGISTER if necessary.
- #7. Read the DATA STRING.



Flow Chart 13-1

NOTE 1: Three (3) is added to #CNTS in order to initialize the counter properly.

80186/8051 INTERFACE DEVICE DESCRIPTION

The primary purposes of the 8051 8-bit processor are:

- #1. Control front panel operation and notify the 80186 of any changes in switch positions.
- #2. Control serial data transfers into and out of the instrument.
- #3. Store ASCII character information and transfer this information to the 80186 upon request.

A communication link with protocol is required for the 8051 processor to "TALK" to the 80186 processor.

The communication link consists of a latched bidirectional 8-bit parallel port and two interrupt lines. Most communication sequences consist of 1 byte, 2 byte, or 3 byte transfers from one processor to the other. Each processor interrupts the other to initiate a communication sequence.

NOTE: The first byte in the transfer is always an "identifier" byte used to identify the type of communication sequence about to take place.

Index 13-1 references the information passed between the two processors.

CHARACTER IDENTIFIER BYTES	INFORMATION	PAGE
1	Initial front panel image	13-24
2	Front panel updates	13-24
4	Serial Data transfers into 320	13-25
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5	Serial Transmission complete	13-26
6	Character string request	13-27
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7	X/Y point transfers	13-28
	Additional Notes About Transfers	13-29
	Summary of 8051 Identifiers	13-29
	320 Character Table	13-30

Index 13-1

INITIAL FRONT PANEL IMAGE

When power is applied to the 320, the front panel controls are scanned to determine their initial positions. This information is conveyed to the 80186 via 18 consecutive bytes. The first byte is an identifier, the next 16 bytes contain the initial control positions, and the last byte is the 8051 version number.

The 8051 interrupts the 80186 with the identifier "1", and then interrupts it again with the first data byte when the 80186 has read the identifier. The 8051 continues to send data bytes as soon as each previous data byte is read by the 80186. This continues until 17 data bytes have been transferred.

FRONT PANEL UPDATES

A two byte transfer to the 80186 occurs for each front panel button and switch position changed.

The 8051 interrupts the 80186 with the identifier '2', and then interrupts it again with a data byte after the 80186 has read the identifier.

The 7 least significant bits of the data byte represent the position in the front panel control matrix where the change took place. The most significant bit represents whether the switch is now open or closed (see Table 13-5).

BIT	SWITCH STATUS
0	Contact Now Open
1	Contact Now Closed

Table 13-5

The 80186 should not act on the changes until it has received all of the changes that occurred on a particular scan. The 8051 notifies the 80186 of the "end of front panel changes" by sending a two byte transfer after all of the changes have been sent. This 2 byte transfer consists of an identifier '2' followed by the number 54 (36 HEX).

SERIAL DATA TRANSFERS INTO THE 320

Serial data transfers that enter into the 320 enter via the serial port on the 8051. A FIFO buffer area in the 8051 has been set up to handle serial data into the 320. This serial information is passed onto the 80186 using a 2 byte transfer.

The 8051 interrupts the 80186 with the identifier '4', and then interrupts it again with a data byte from the buffer after the identifier has been read by the 80186.

SERIAL ERRORS

The buffer may overflow, causing lost information, if the transfer rate from the 8051 to the 80186 is too slow.

The 8051 monitors this condition and sets an error flag internally if it occurs, notifying the 80186 with a 1 byte transfer of identifier '3'.

NOTE: This is mainly for diagnostic purposes to help determine if there are any limitations on serial transfer rate into the 320.

SERIAL DATA TRANSFER OUT OF THE 320

A two byte transfer is initiated by the 80186 when serial data is to be transferred out of the 320.

The 80186 interrupts the 8051 with the identifier '4', then monitors the status of D8 (bit 9 of the 16-bit data bus) to determine when the second byte of the two byte transfer can be sent. See Table 13-6.

D8	STATUS
Logic 1	Parallel port is busy, the 80186 must wait.
Logic 0	The 80186 can send the second byte.

Table 13-6

SERIAL TRANSMISSION COMPLETE

Once the 8051 has received a data byte for transfer out of the 320, the 8051 tests the clear to send (CTS) line and tests for XOFF.

If conditions are okay to transfer, the 8051 will start the serial transmission. The 8051 notifies the 80186 with a 1 byte transfer of the identifier '5' when the transmission is complete.

NOTE: The 80186 must receive identifier '5' before it will attempt to transmit any more characters out the serial port.

CHARACTER REQUEST

When the 80186 requires character information from the 8051, it initiates the action with a two byte transfer to the 8051.

The 80186 interrupts the 8051 with the identifier '6', and then monitors D8 until it goes to a logic 0 before sending the second byte.

NOTE: The second byte must be the ASCII code for the character desired.

POINT REQUEST

The 80186 requests the next point of a character string by interrupting the 8051 with a one byte transfer of the identifier '7'. The 8051 responds with the three byte transfer outlined in the "X/Y Point Transfer" discussion. This handshaking takes place until all points of the character string have been transferred.

X/Y POINT TRANSFER

When the 8051 has received either a character request or a point request from the 80186, the 8051 responds with a three byte transfer to the 80186.

The 8051 interrupts the 80186 with the identifier '7', and then interrupts the 80186 with the X-coordinate of a character "point" after the 80186 has read the identifier.

NOTE: Point refers to an actual dot on the CRT for a character being displayed. A point therefore requires both an X- and a Y-coordinate.

After the X-coordinate has been read by the 80186, the 8051 interrupts the 80186 with the Y-coordinate of the character point.

NOTE: A Y-coordinate equal to (or greater than) 128 signifies the last point in the character string. If the point currently being transferred to the 80186 is not the last point of the character string, the 80186 must request the next point of the string as outlined in "Point Request."

ADDITIONAL NOTES ABOUT TRANSFERS

#1. Whenever multibyte transfers are initiated (such as 3 byte point transfers from the 8051, or character requests from the 80186), the transfer sequence currently in progress must be completed before another can begin.

Once a transfer sequence has been completed, any other type of transfer sequence can take place.

#2. The 80186 must be able to read the status of the parallel port when involved in multibyte transfers. It must also be able to read data sent to it by the 8051 via the parallel port.

Address line A1 is used to distinguish between the two read operations (see Table 13-7).

A1	INFORMATION READ
Logic 0	Data is read
Logic 1	Status is read

Table 13-7

SUMMARY OF THE 8051 IDENTIFIERS

#1. Initial Front Panel Image

#2. Front Panel Update

#3. Serial Error (Buffer Overflow)

#4. Serial Data (Transmit/Receive)

#5. Serial Transmission Complete

#6. Character Request

#7. Point Request/Transfer

320 CHARACTER TABLE

CHAR	HEX	DEC	NS	CHAR	HEX	DEC	NS	CHAR	HEX	DEC	NS
SP	20	32		@	40	64		←	60	96	!
!	21	33		A	41	65		a	61	97	
"	22	34		B	42	66		b	62	98	
#	23	35		C	43	67		c	63	99	
\$	24	36		D	44	68		d	64	100	
%	25	37		E	45	69		e	65	101	
&	26	38		F	46	70		f	66	102	
'	27	39		G	47	71		g	67	103	
(	28	40		H	48	72		h	68	104	
)	29	41		I	49	73		i	69	105	
*	2A	42		J	4A	74		j	6A	106	
+	2B	43		K	4B	75		k	6B	107	
,	2C	44		L	4C	76		l	6C	108	
-	2D	45		M	4D	77		m	6D	109	
.	2E	46		N	4E	78		n	6E	110	
/	2F	47		O	4F	79		o	6F	111	
0	30	48		P	50	80		p	70	112	
1	31	49		Q	51	81		q	71	113	
2	32	50		R	52	82		r	72	114	
3	33	51		S	53	83		s	73	115	
4	34	52		T	54	84		t	74	116	
5	35	53		U	55	85		u	75	117	
6	36	54		V	56	86		v	76	118	
7	37	55		W	57	87		w	77	119	
8	38	56		X	58	88		x	78	120	
9	39	57		Y	59	89		y	79	121	
:	3A	58		Z	5A	90		z	7A	122	
;	3B	59		[	5B	*		±	7B	123	!
<	3C	60		\	5C	*		°	7C	124	!
=	3D	61		]	5D	*		Ω	7D	125	!
>	3E	62		^	5E	94		∞	7E	126	!
?	3F	63		_	5F	*		μ	7F	127	!

Table 13-8

CHAR = Characters list.

HEX = Hexadecimal equivalents.

DEC = Decimal equivalents. (A "*" in this column indicates unimplemented characters.)

NS = Non-standard (non-ASCII) characters identified with a "!".

NOTE: An attempt to print an unimplemented character, or one not in the above table results in a question mark "?" being printed.

THE 320 DISPLAY SYSTEM

This section is provided to explain the process of displaying data on the screen.

From the programmer's point of view the display system is a memory area which retains a list of the X,Y coordinates of each waveform or character on the display CRT. There is also an I/O control port which controls the special features of the display system.

The display system hardware sequences through the list of coordinates, decodes the control bits, and generates the analog signals needed to drive the display amplifiers and the CRT cathode.

THE DISPLAY RAM

To the programmer, the display RAM looks like 32K words of memory, 12 bits wide each (i.e., the lower 4 bits of each standard 16 bit word are not active). The most significant 10 bits of each word represent either the X- or the Y-coordinate of a point on the CRT.

The X-Coordinates

The X-coordinates are stored in memory addresses 10000 through 17FFF.

The additional 2 data bits associated with the 10-bit X-coordinate control the intensity of the point to be displayed. These are referred to as the beam bits (b1, b0).

The intensity of a point on the screen follows in natural order the binary sequence:

00 = dark

01 = low intensity

10 = medium intensity

11 = high intensity

The Y-Coordinates

The Y-coordinates are stored in memory addresses 18000 through 1FFFF.

The additional 2 data bits associated with the Y-coordinate control are referred to as the mode bits (m1, m0). The mode bits alter the function of the beam bits.

Of the four possible modes, three have been defined.

10 = ON mode. The beam bits operate as they have been described with no alteration or conditions.

01 = OFF mode. The beam will remain off or dark under all circumstances.

00 = NORM mode. The beam will operate normally only when a "match" condition does not exist. If a match condition exists, then the beam will be forced off or dark.

The I/O control register contains eight bits that represent eight sections in the display memory space. A "match" is indicated if the point currently being displayed is in a section whose bit is set.

That is, the control register can signal a match in none, one, ... up to all eight sections of the display RAM. This allows an entire waveform to be turned off with the "flick" of one bit in the control register. In this way a section of memory may be "turned" dark while a new waveform is built and then turned on again.

11 = Not used at this time.

THE I/O CONTROL REGISTER

The I/O control register has three control bits in addition to the eight match bits just mentioned.

The match bits reside in the upper eight positions in the word.

Bit 7 - The YTG bit controls the X-gain of the display amplifiers. This is needed to properly display data in the XY mode. In the normal YT display mode, the aspect ratio of the display is 10:8 as is a standard oscilloscope.

It is desirable to have an aspect ration of 1:1 when displaying one waveform against another, as in the XY mode. Therefore, the YTG bit reduces the gain of the X-amplifier so that the 1:1 ratio is attained.

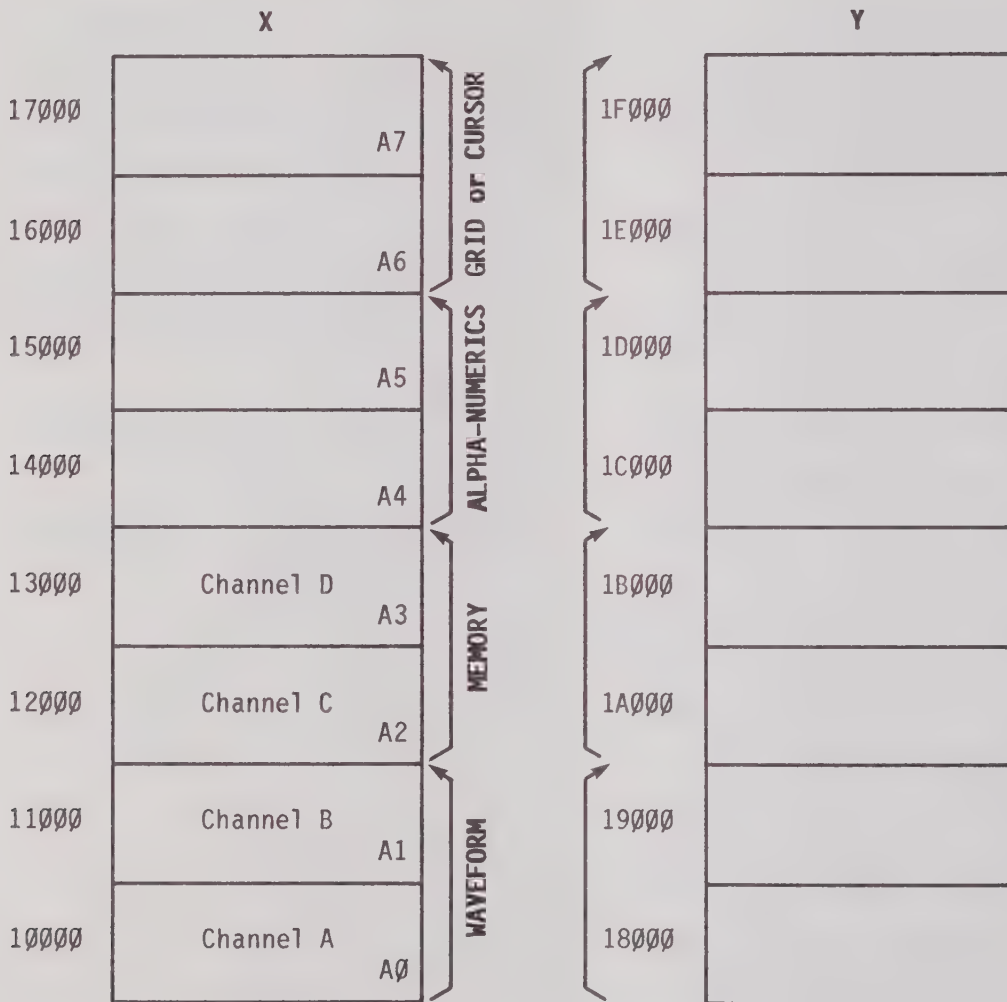
Bit 6 - Bit 6 is a master beam kill bit. This bit will disable all the points on the screen.

Bit 5 - Bit 5 is used to lift the pen of the external plotter (if one is attached and in use).

Bit 1 - Bit 1 is used to enable/disable the beeper.

Bit 0 - The YTG- bit is the inverse of the YTG bit.

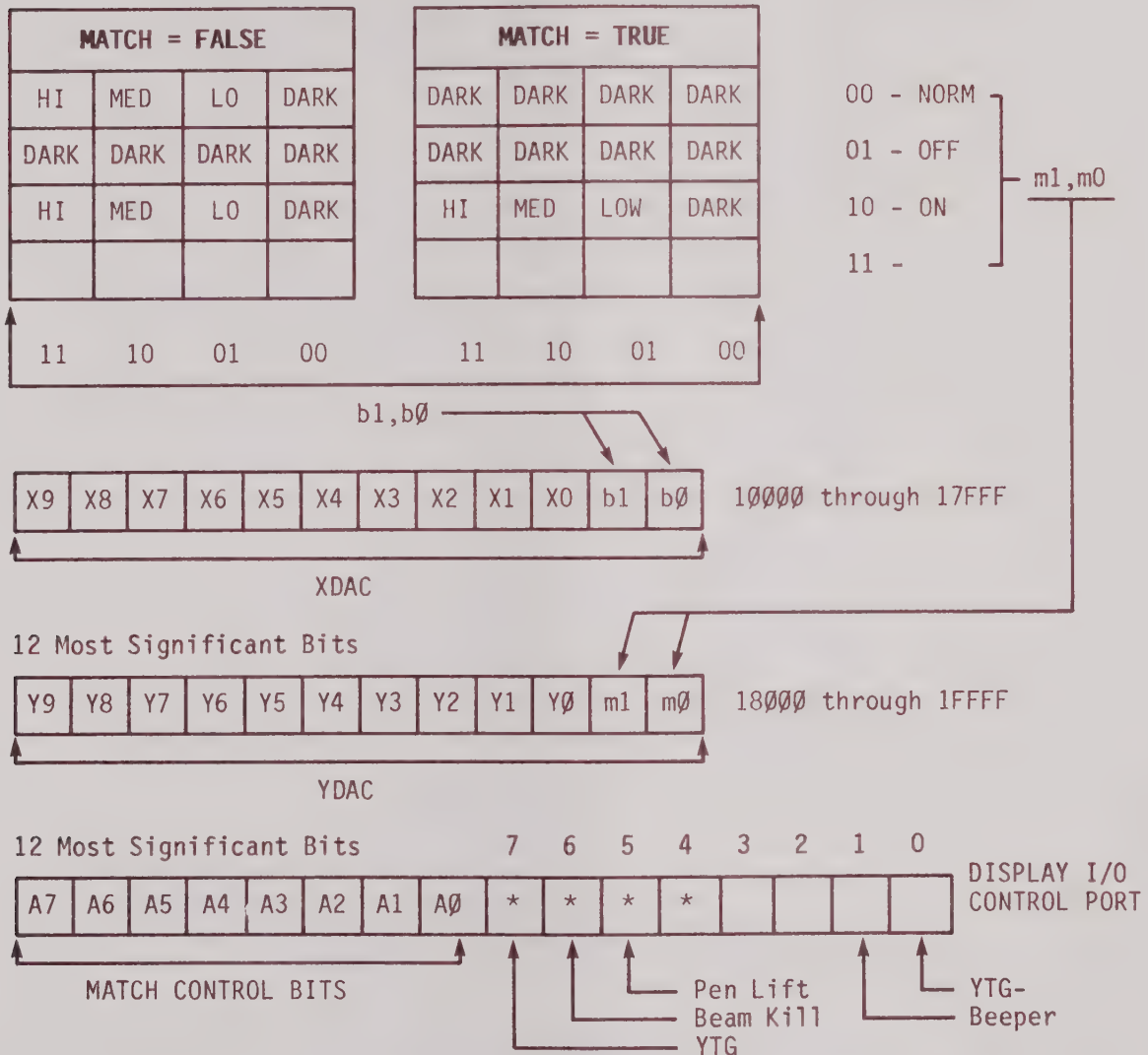
TYPICAL DISPLAY - MEMORY MAP



MATCH BIT corresponding to this block. See page 13-35.

NOTE: There are 16,384 display points available. Each point is located on the screen by a 2 byte X and 2 byte Y position as indicated in the above diagram.

BIT POSITIONS AND FUNCTIONS



If in NORM display ($m1, m0 = 00$) and the MATCH BIT corresponding to the block that this X,Y pair is from (see previous page) is true ($=1$), this dot will be DARK. However, if the MATCH BIT is false ($=0$), the dot intensity is determined by $b1, b0$ (HI, MED, LO, DARK).

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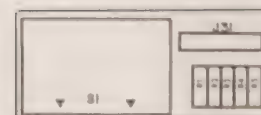
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NOTE #1: The External Control board accessory is not available at this time.

NIC-320 SCHEMATICS AND COMPONENT PLACEMENTS

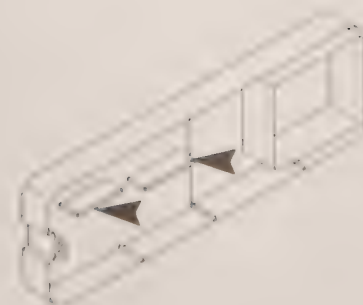


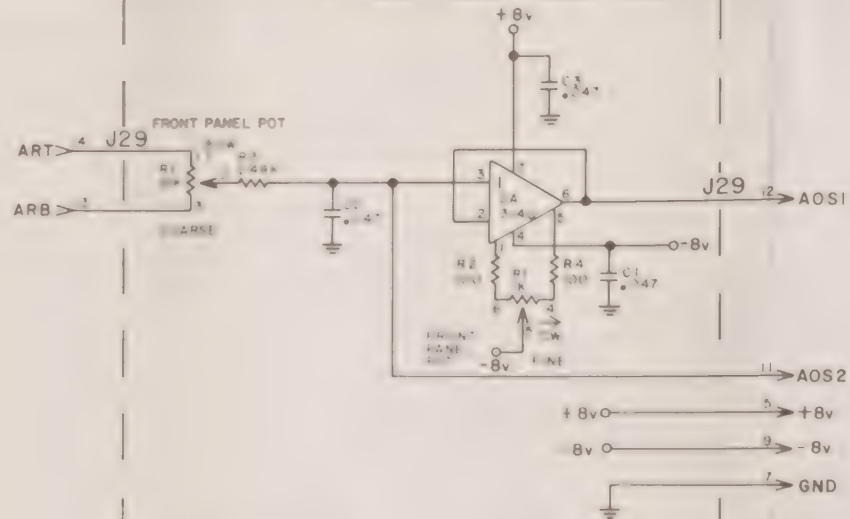
DC OFFSET POT BOARD



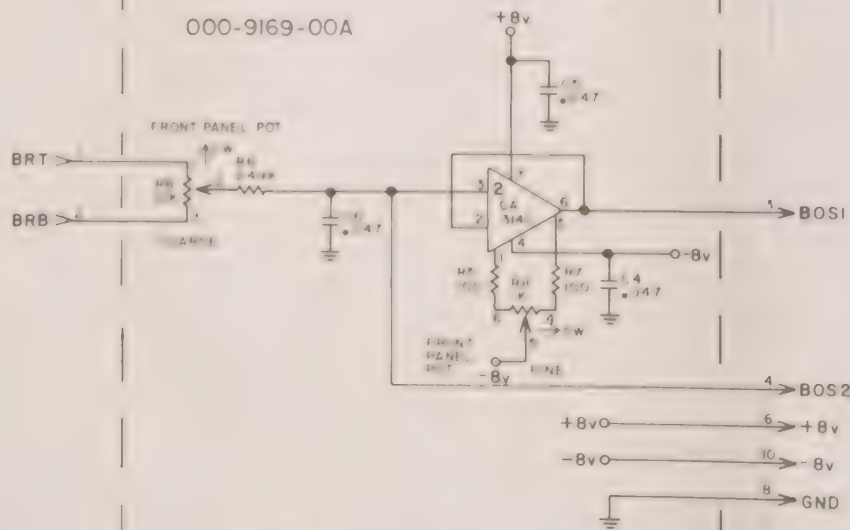
TIME PER POINT BOARD

NIC-320 DC OFFSET POT BOARD
000-9169-00A
NIC-320 TIME PER POINT BOARD
000-9168-01A

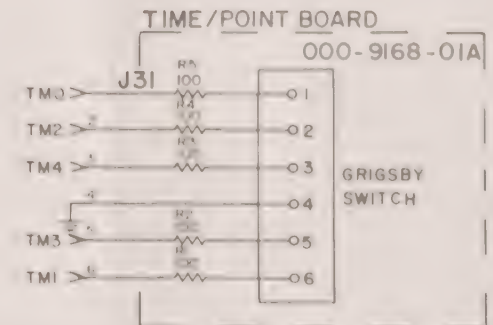




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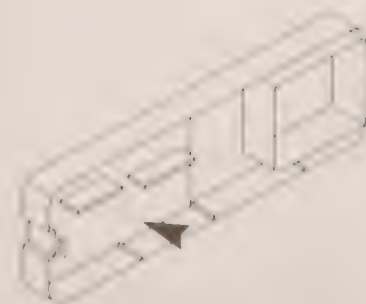
DC OFFSET POT BOARD

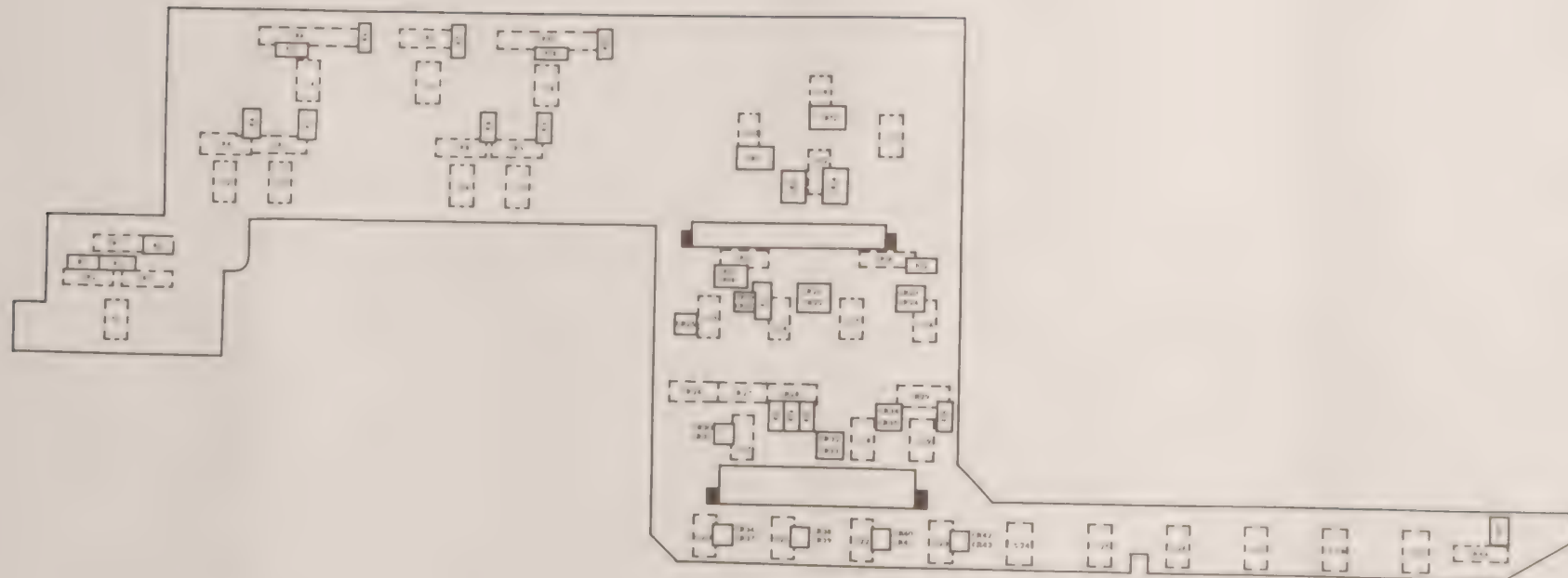


NICOLET INSTRUMENT CORP
3XX DC OFFSET POT &
TIME/POINT BOARDS
000-916801A & 000-916900A
JJH
3-6-85

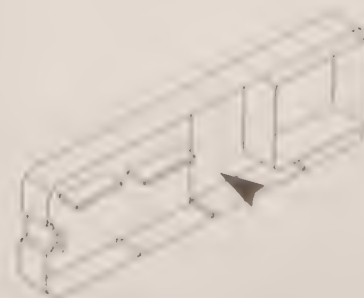


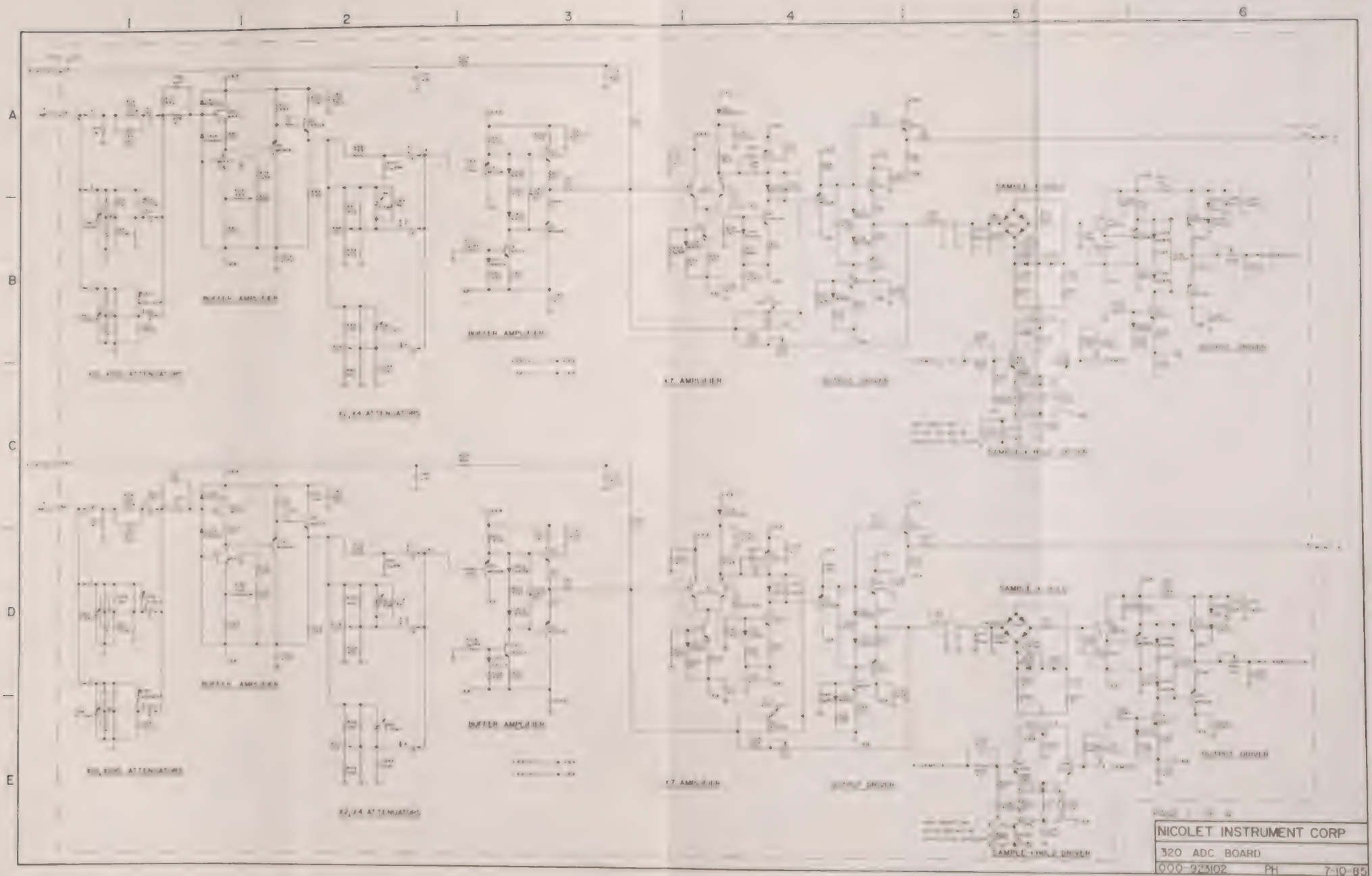
MIC-320 TRIGGER BOARD
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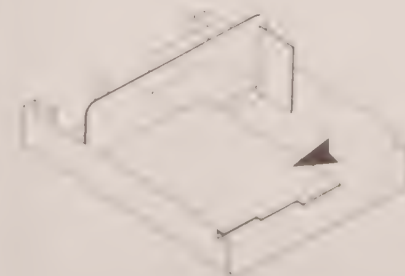
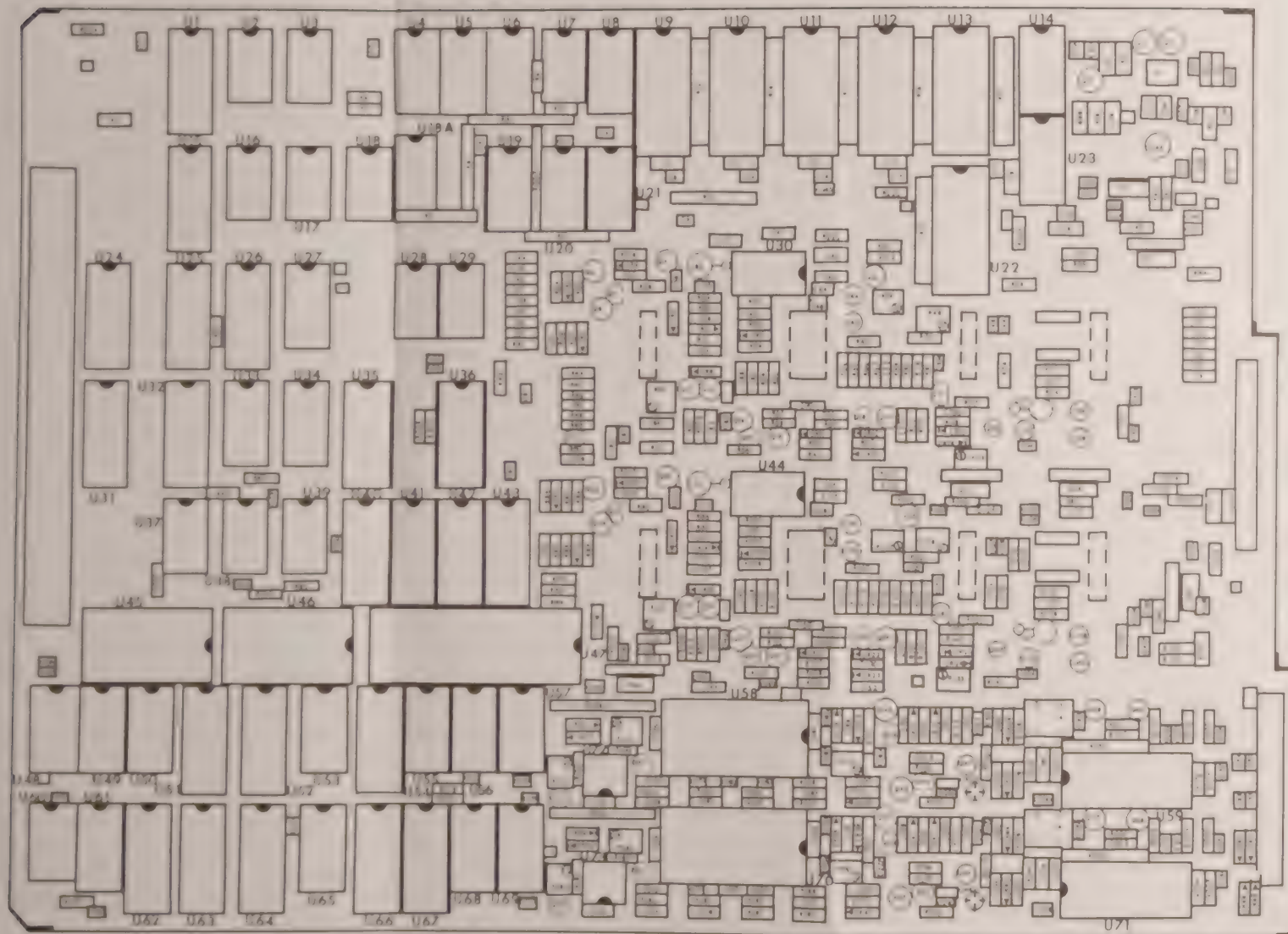




MIC-320 CURSOR BOARD
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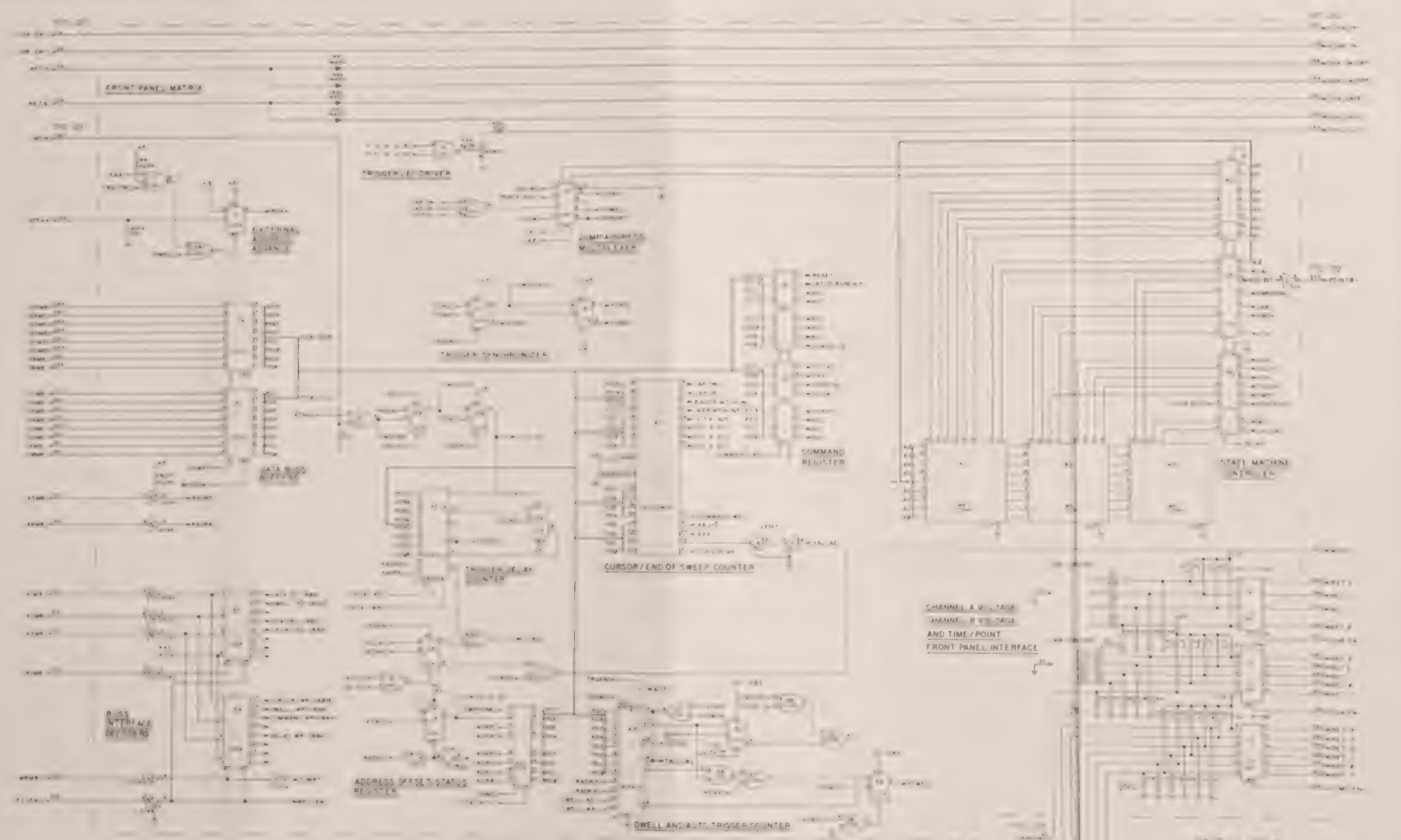




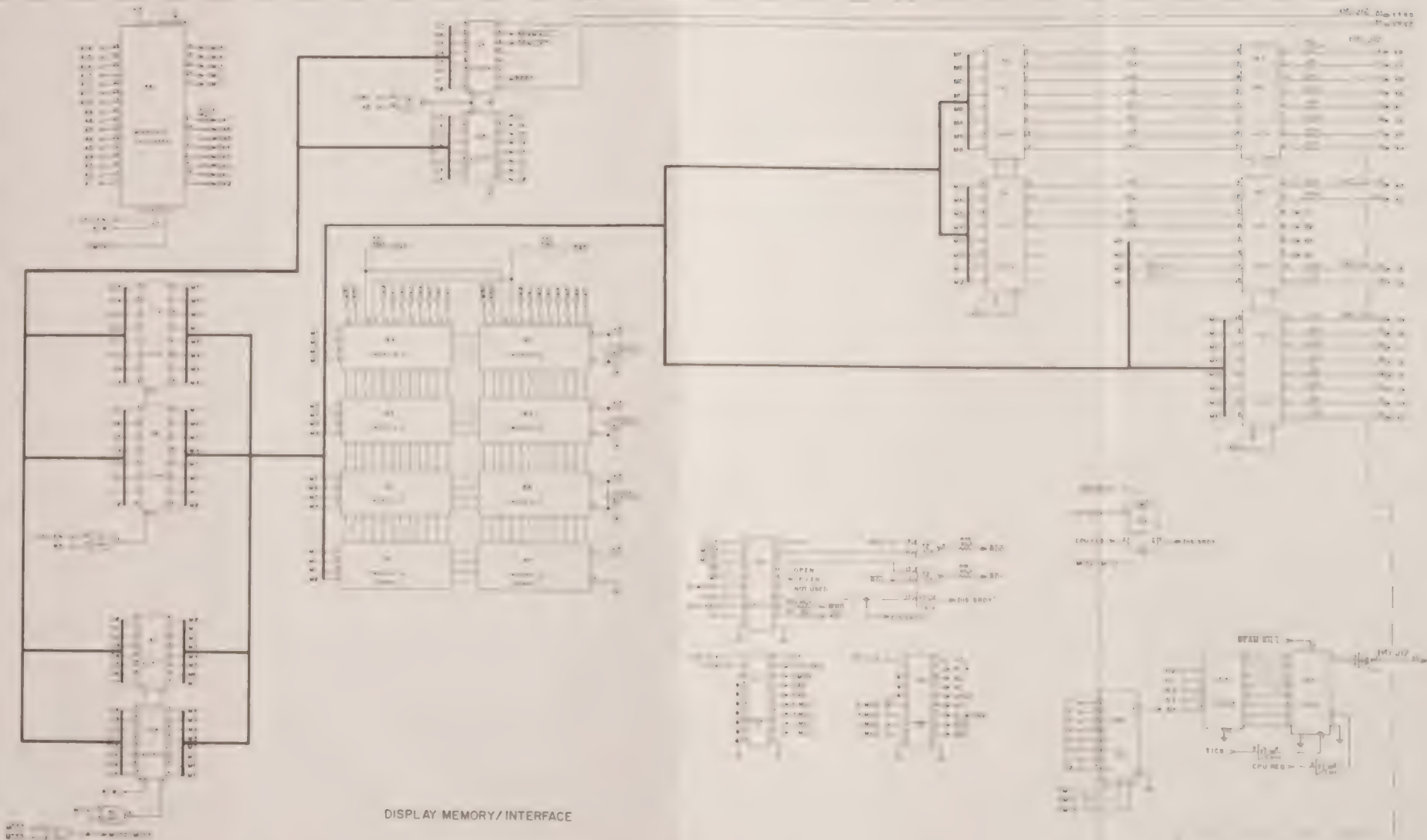


NIC-320 ADC BOARD
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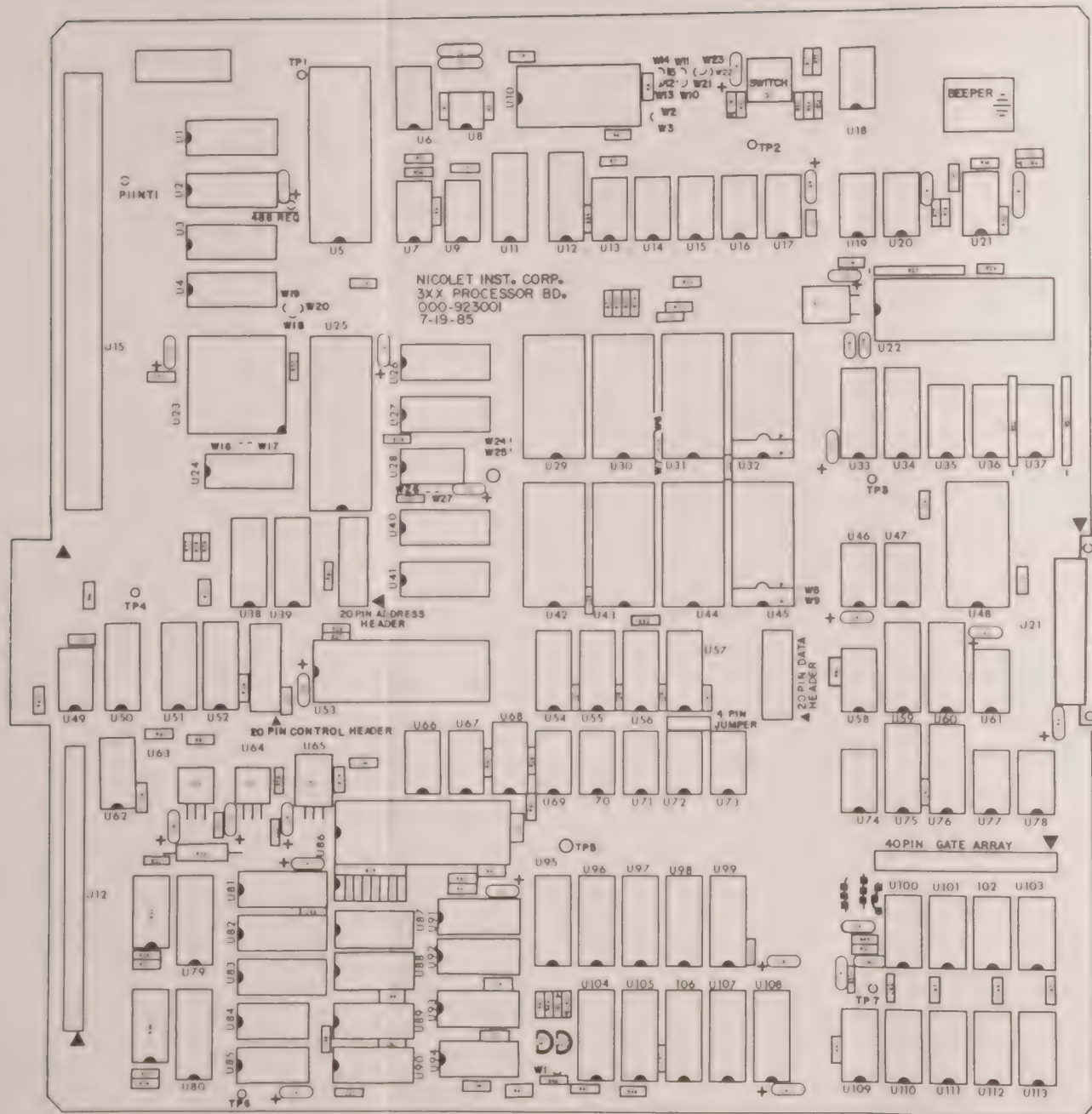
A
B
C
D
E



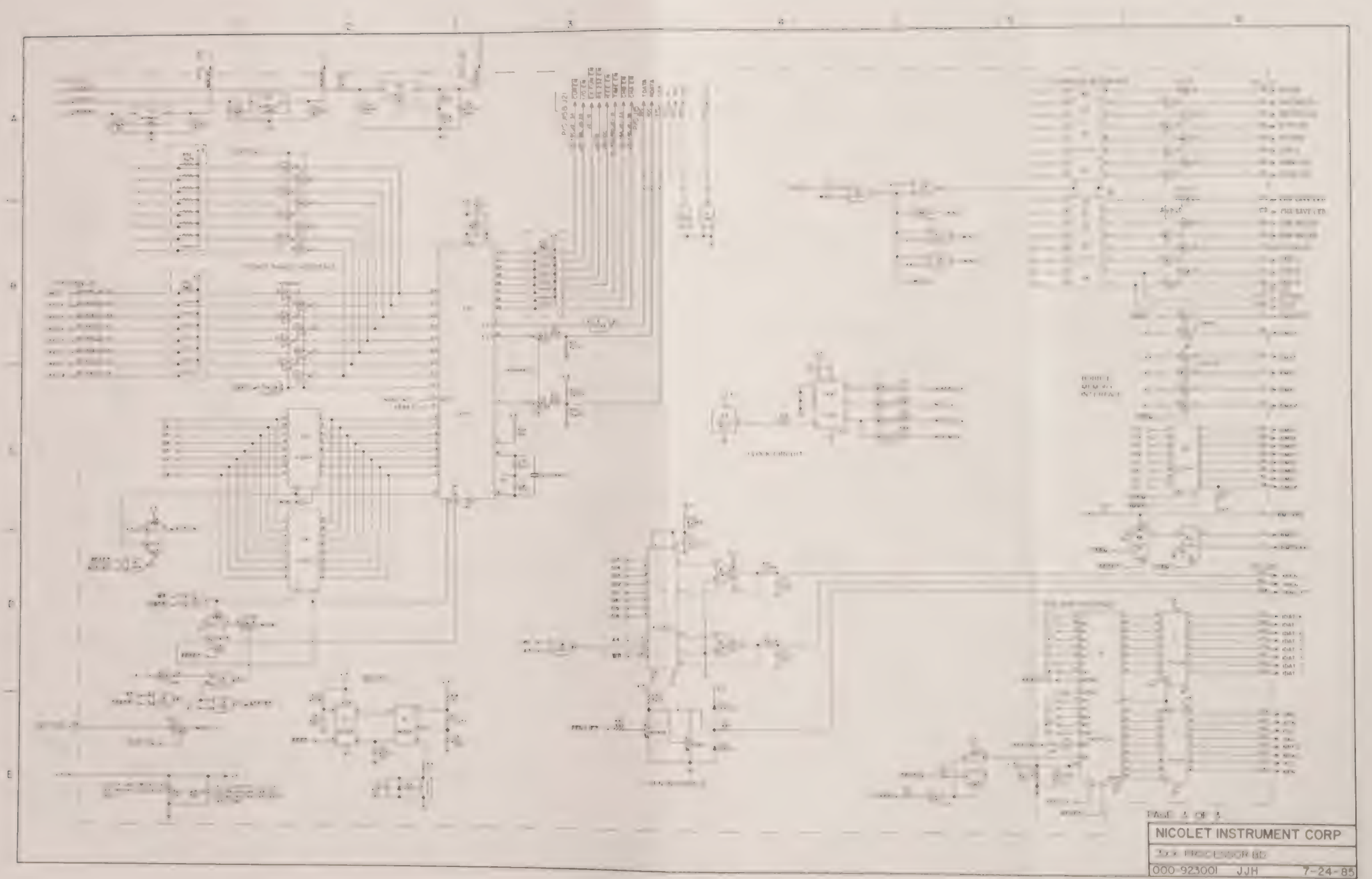
A
B
C
D
E



DISPLAY MEMORY/INTERFACE



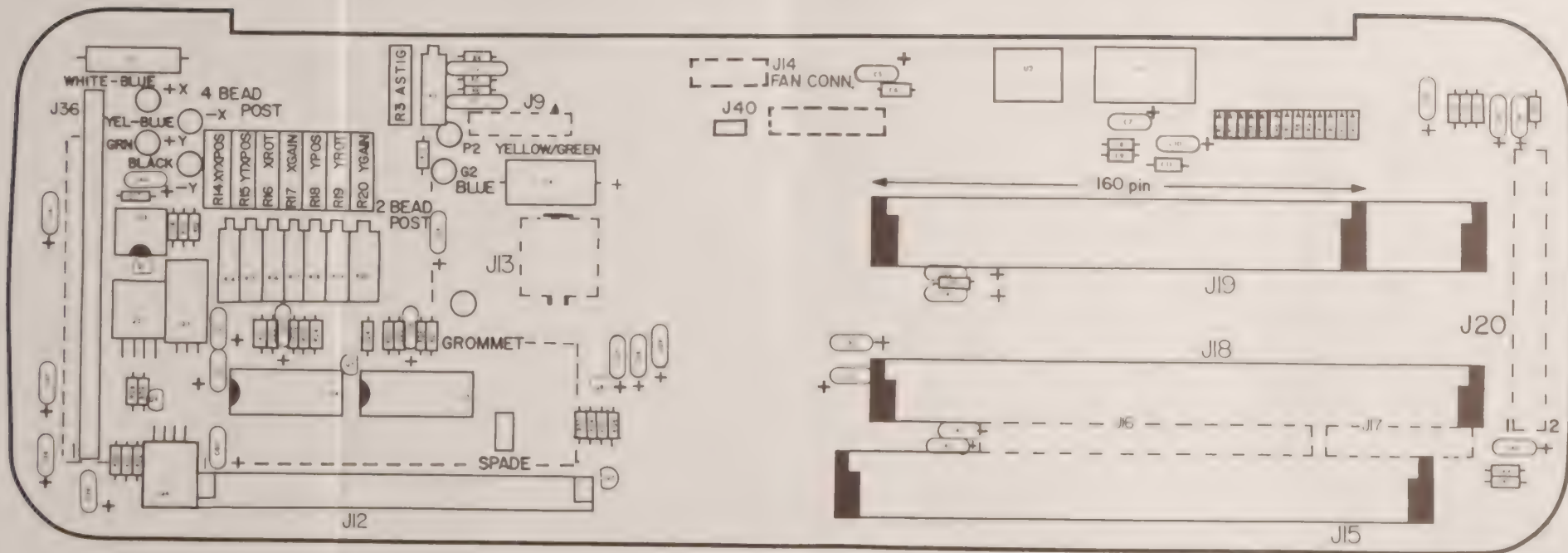
NIC-320 PROCESSOR BOARD
000-9230-01



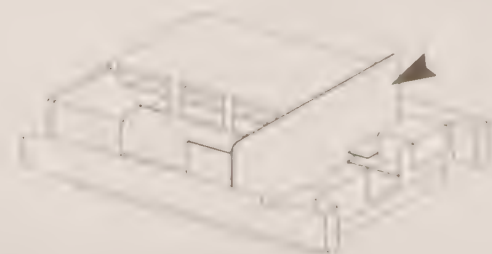
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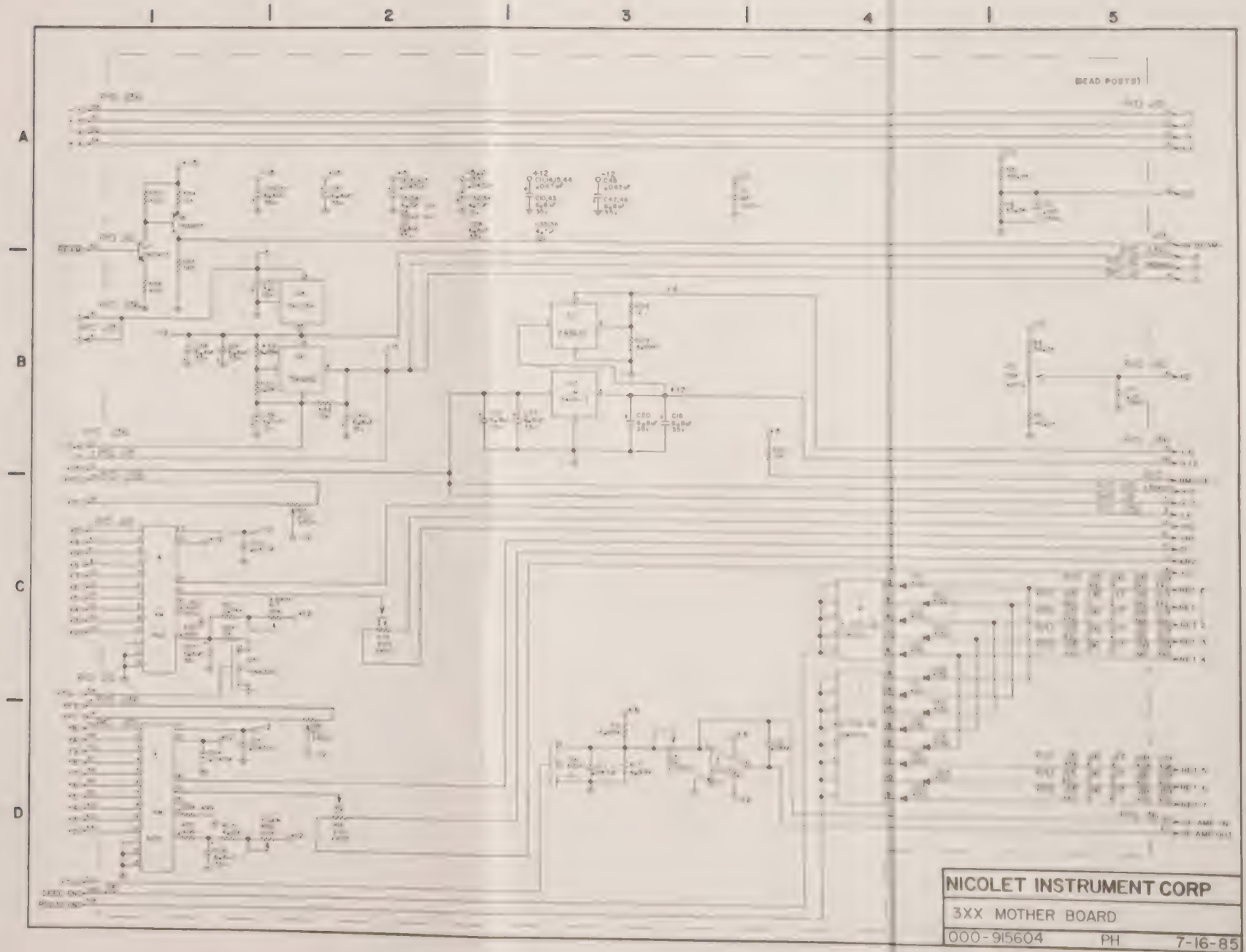
CLOCK CIRCUIT

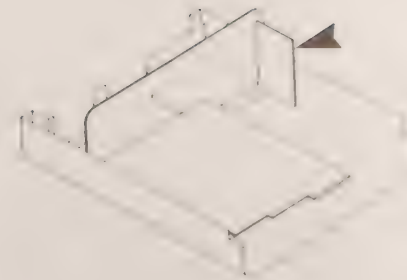
BOARD 1
OF 2
IN THE SET



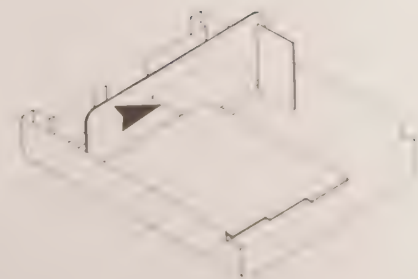
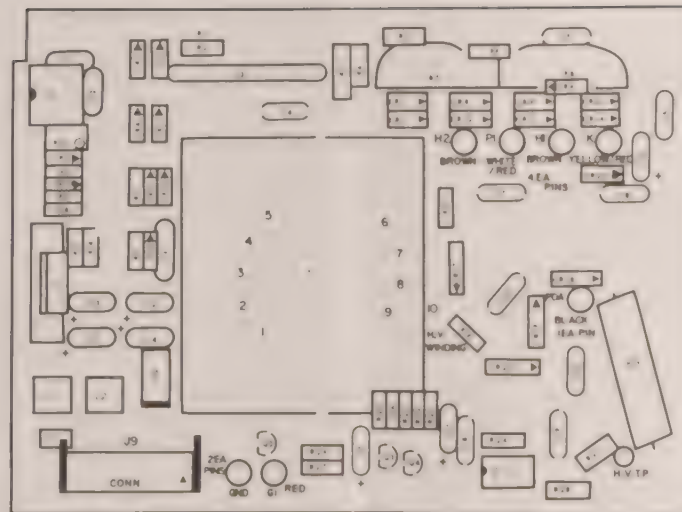
NIC-320 MOTHER BOARD
000-9156-04



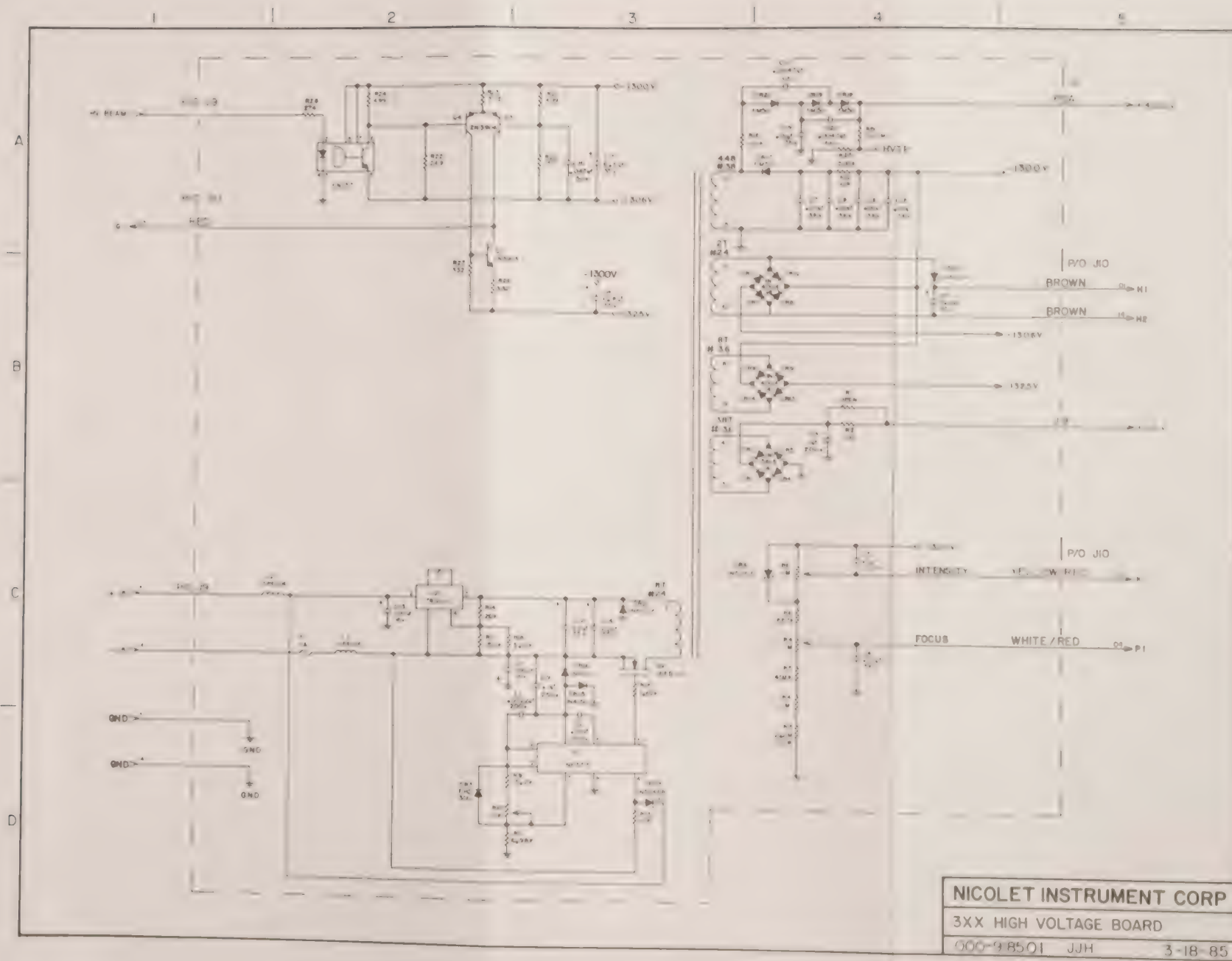




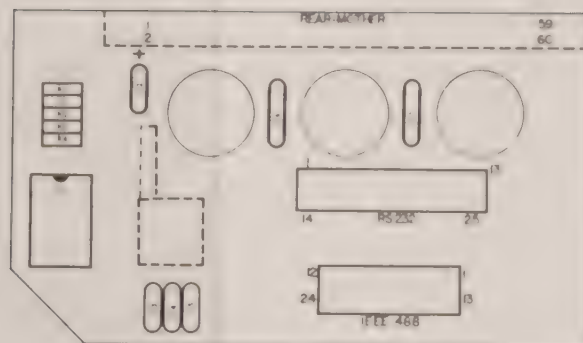
14-26



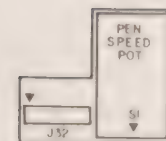
MIC-320 HIGH VOLTAGE BOARD
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NICOLET INSTRUMENT CORP
 3XX HIGH VOLTAGE BOARD
 000-918501 JJH 3-18-85



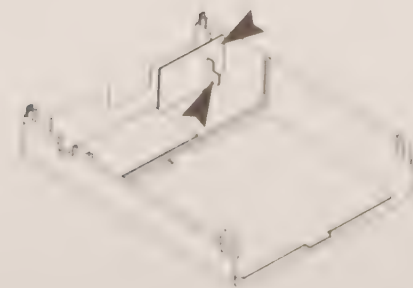
REAR PANEL BOARD



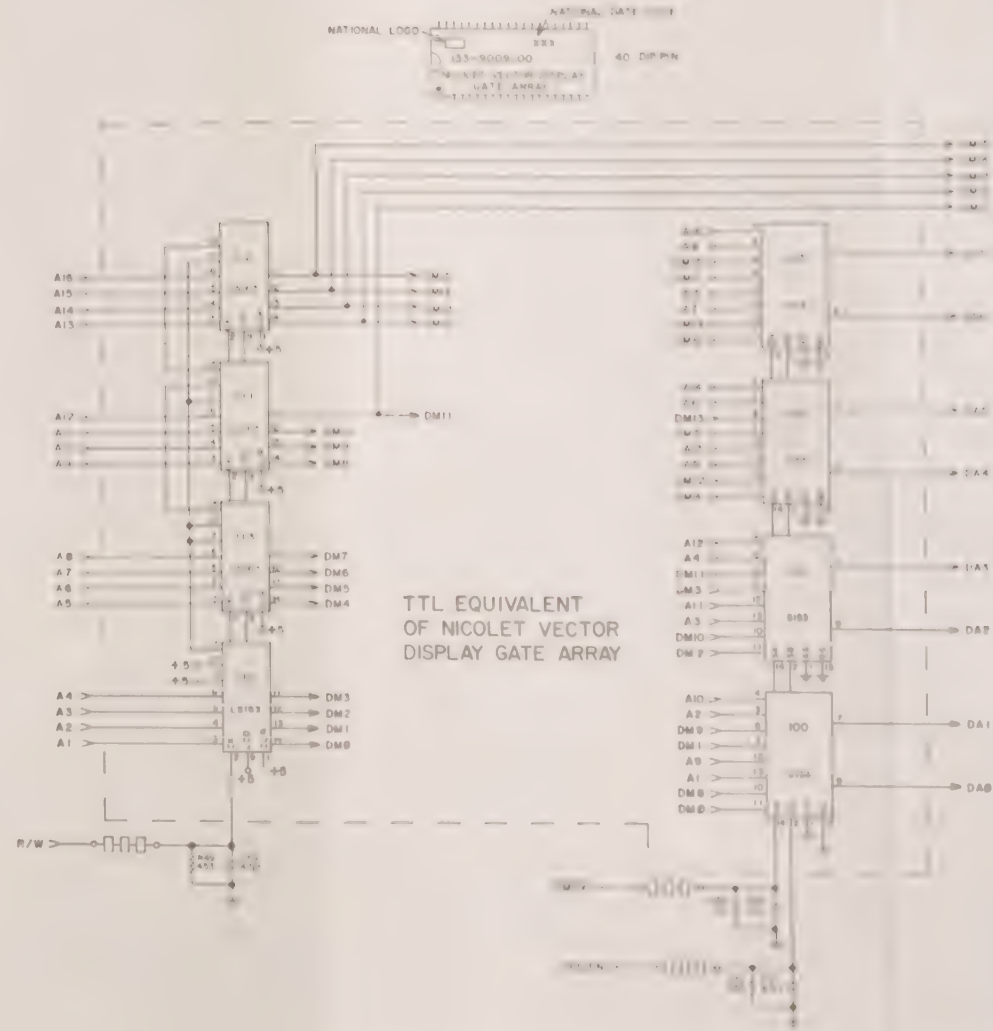
PEN SPEED POT BOARD

NIC-320 REAR PANEL BOARD
000-9158-01A

NIC-320 PEN POT BOARD
000-9159-01



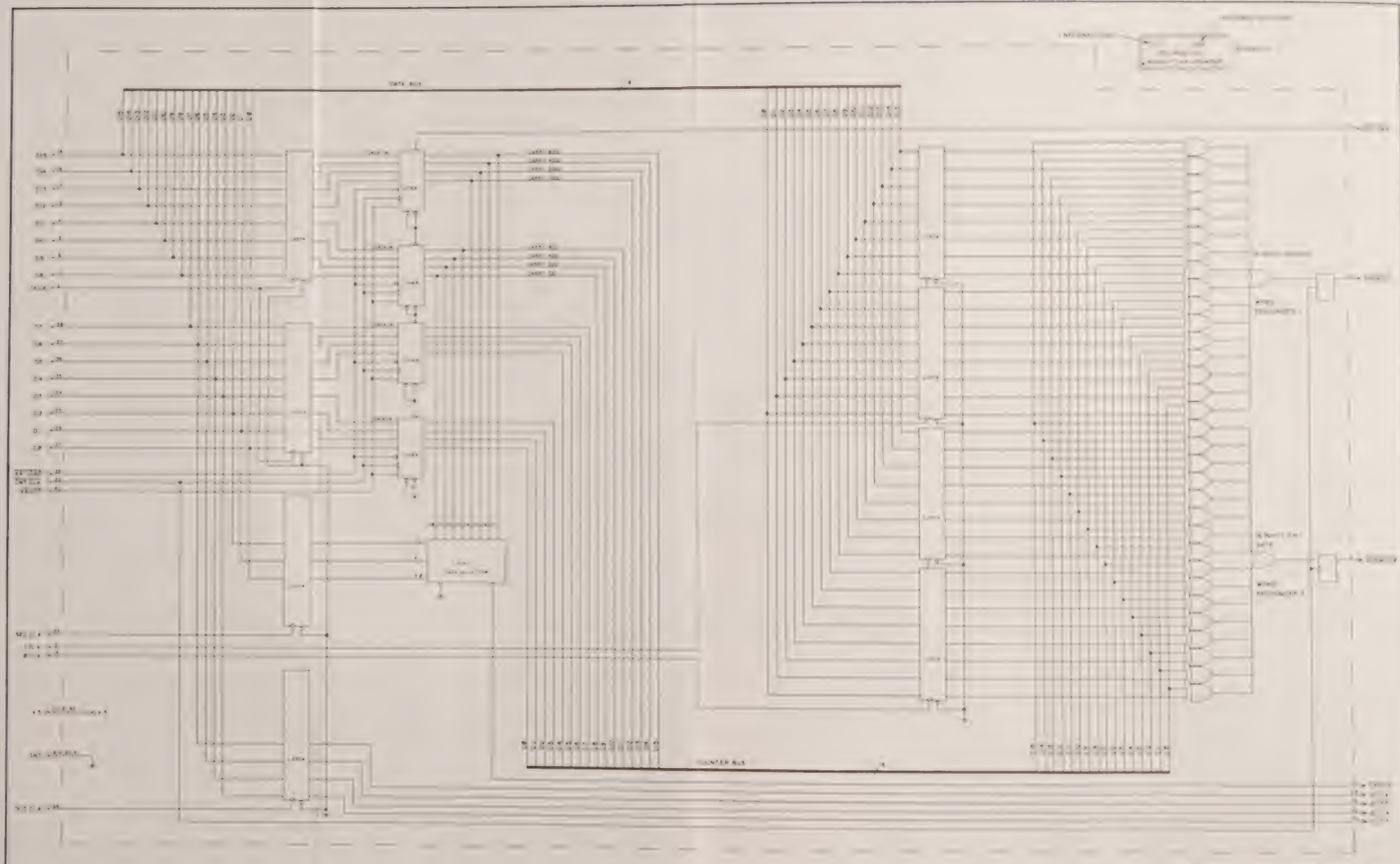
BLANK PAGE



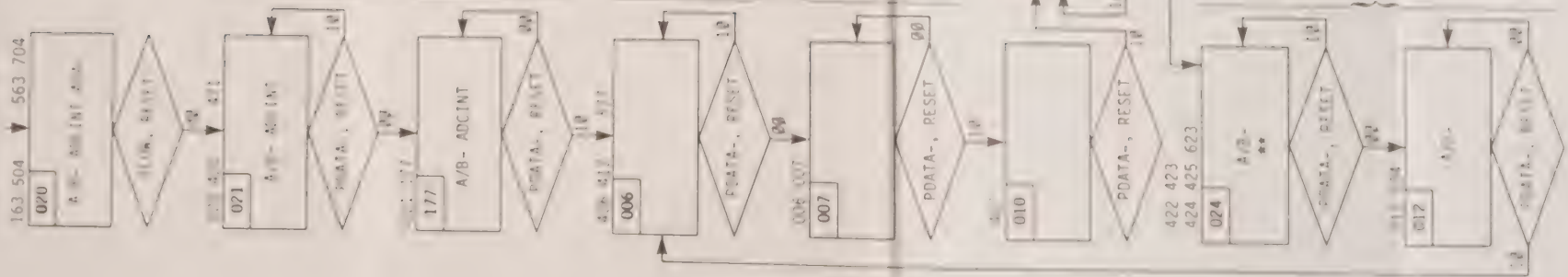
NICOLET INSTRUMENT CORP

NICOLET VECTOR DISPLAY GATE ARRAY

133-9009-00 PH 6-14-84

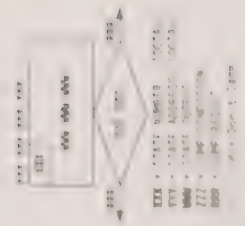


FROM STATE 104 OR 163

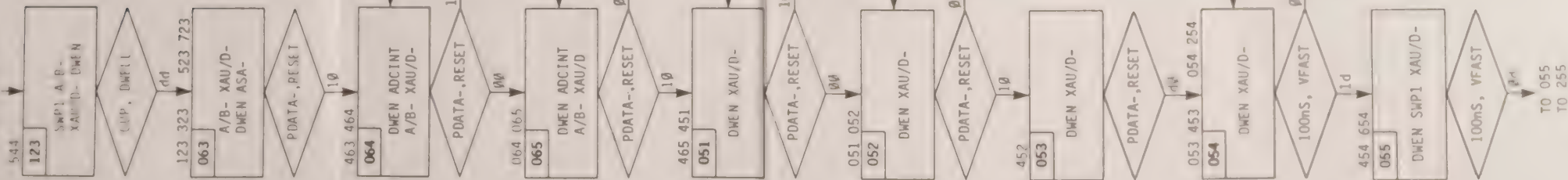


** STATE MACHINE WILL STAY IN THIS STATE AT THE END OF THE BURST-MODE DUMP.

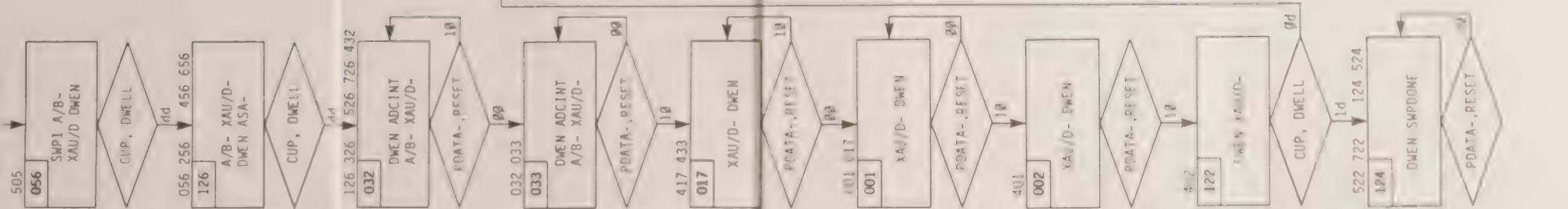
BURST MODE DUMP FROM ADC BUFFER MEMORY TO PROCESSOR WAVEFORM MEMORY



FROM STATE 144



FROM STATE 105



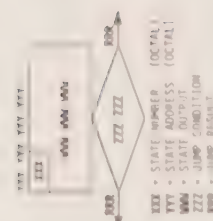
DECREMENT SA ADDRESS

DUMP POINT FROM CHANNEL A

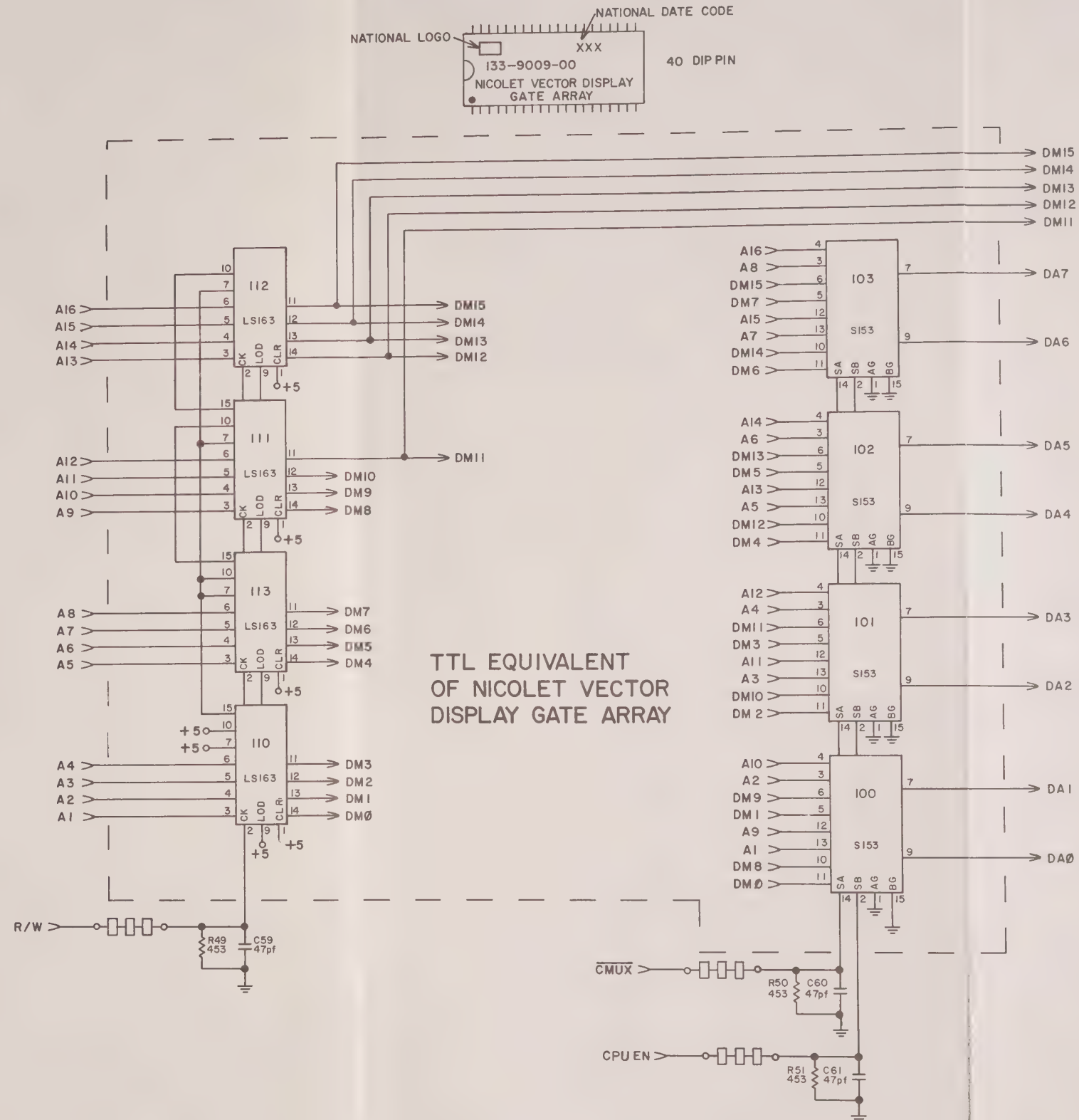
DUMP POINT FROM CHANNEL B

RESYNCHRONIZE

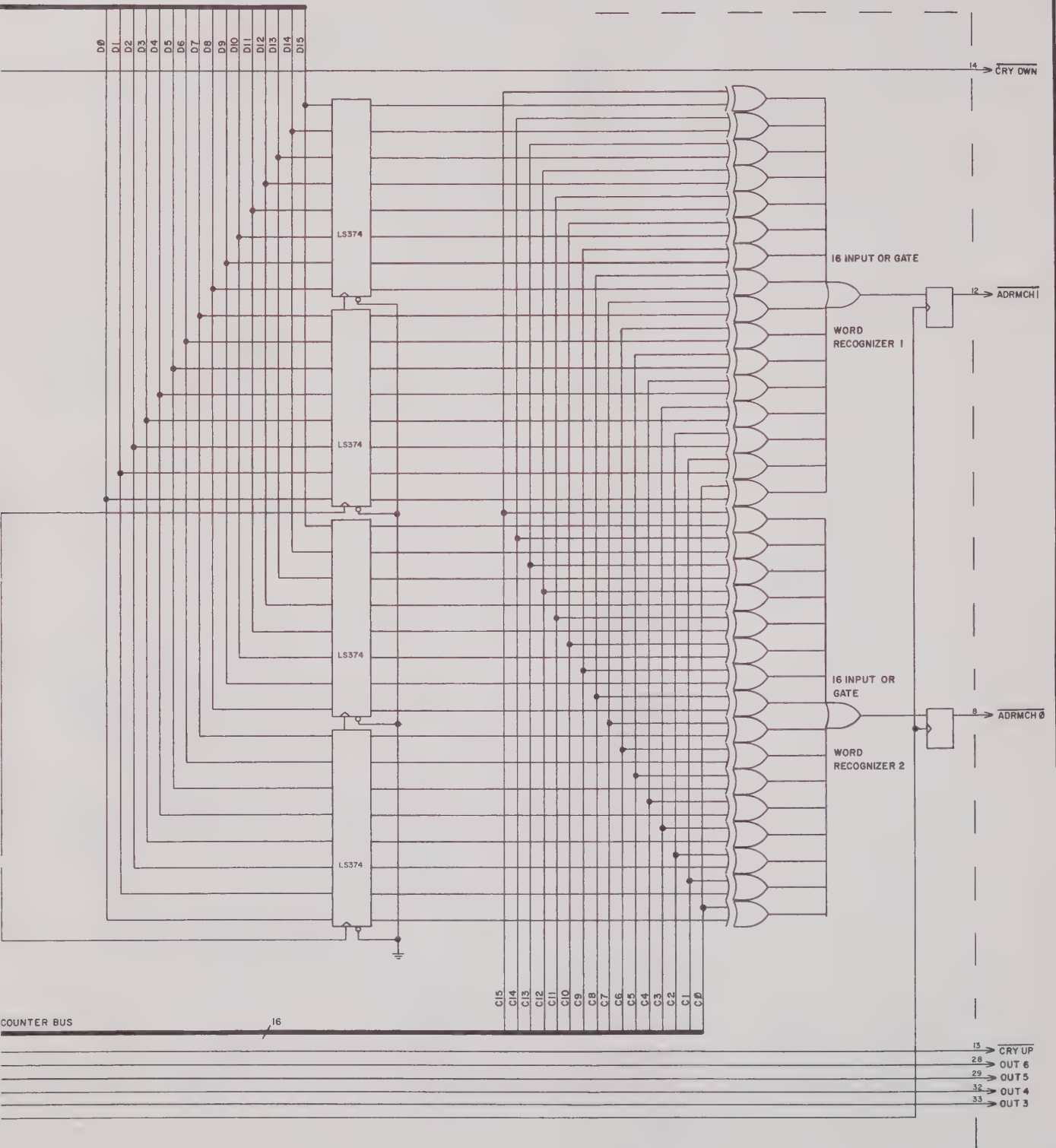
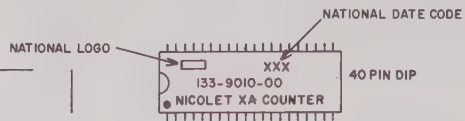
CHECK FOR END OF SWEEP



POINT BY POINT DUMP FROM ADC BUFFER MEMORY TO PROCESSOR WAVEFORM MEMORY



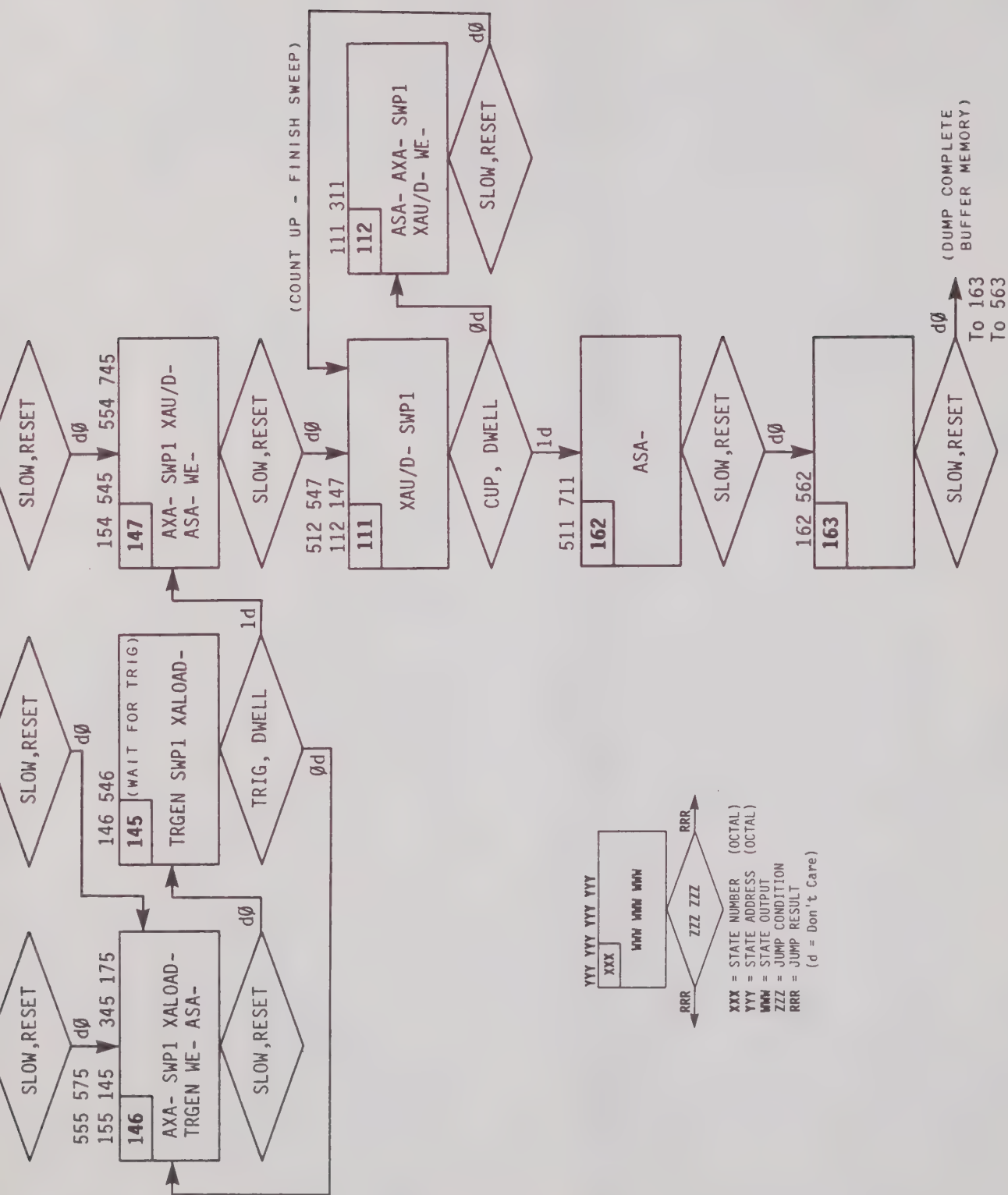
NICOLET INSTRUMENT CORP
 NICOLET VECTOR DISPLAY GATE ARRAY
 133-9009-00 PH 6-14-84



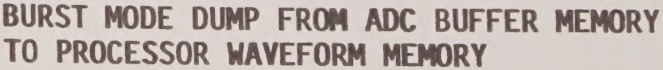
NICOLET INSTRUMENT CORP

XA COUNTER GATE ARRAY

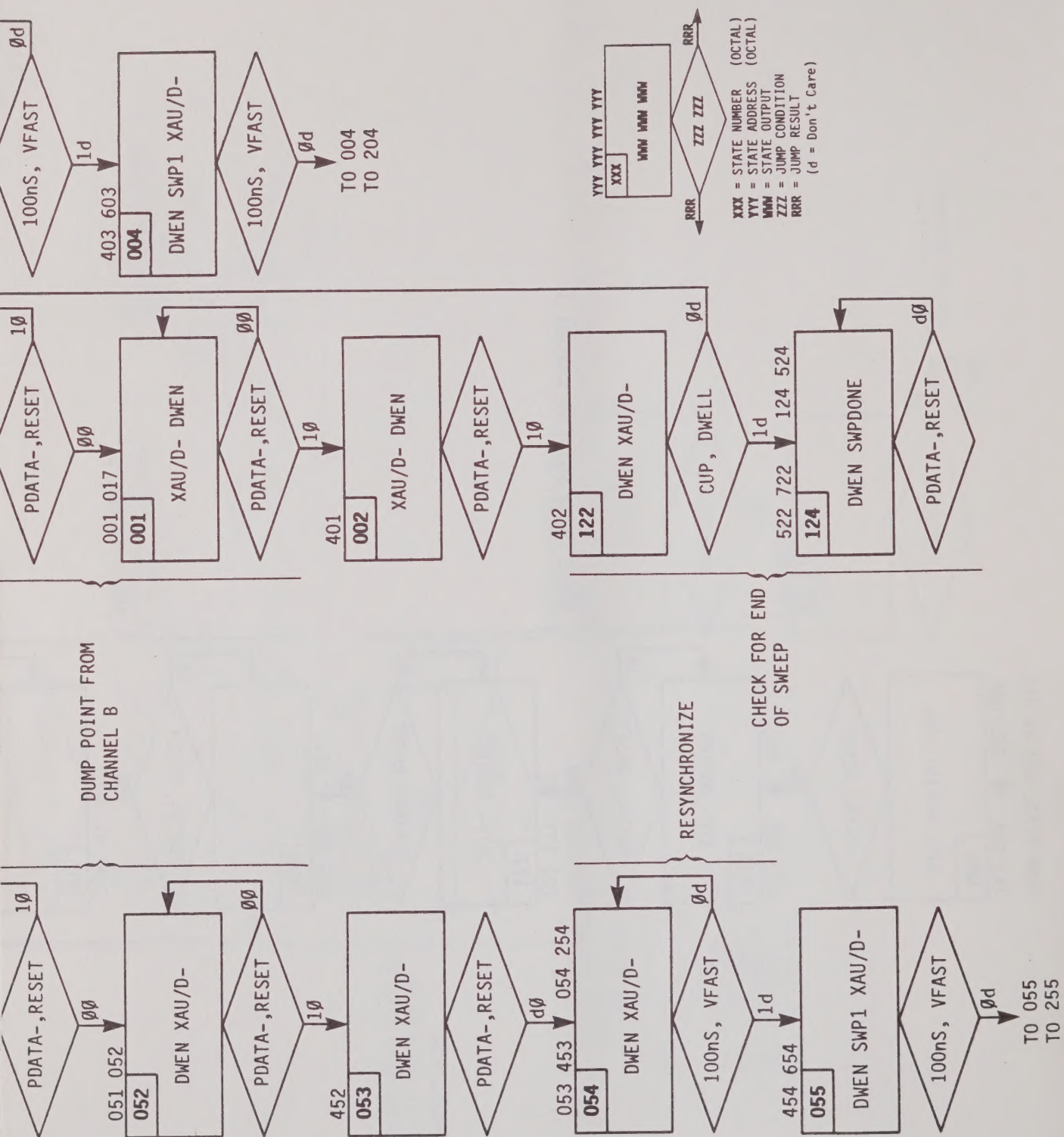
133-9010-00 JJH 6-14-84



VFAST AND SAMPLING
 (Time Per Point = 100nS or Faster)
 FILL BUFFER MEMORY



POINT BY POINT DUMP FROM ADC BUFFER MEMORY TO PROCESSOR WAVEFORM MEMORY





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